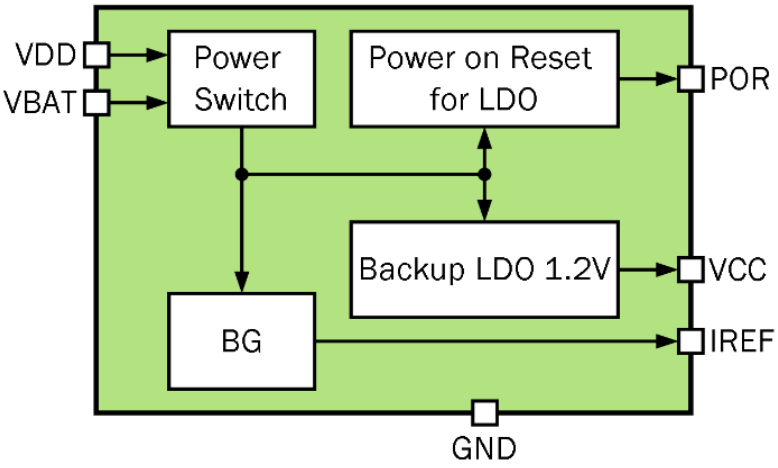
Power management unit (1.2 V output voltage, 945 nA output current)

OVERVIEW



065TSMC_PMU_01 is designed to supply embedded integrated circuits with stable and precise internal voltage and currents. It integrates power switch element, LDO, Bangap and Power On Reset block. PMU have controllable input voltage level and are complemented with VDD detectors to monitor the input voltage value. Two modes are available: full power mode and battery mode. If IO power voltage enable then LDO supply powered by 2.5V, if IO power voltage disable then LDO supply powered by battery power. The voltage regulator consists of a differential amplifier which compares reference voltage with voltage from a feedback divider. It adjusts the impedance of a PMOS transistor for stabilization of output voltage at a set level. PMU have Power On Reset block which generate logic level signal to control LDO power supply.

IP technology: TSMC CMOS 65nm.

IP status: silicon proven.

Area: 0.094mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Power supply	V_{DD}	-	2.25	2.5	2.75	V
Battery power supply	V_{BAT}	Battery mode	0.9	-	1.6	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Output voltage	V_{CC}	V_{DD}=2.5V, external capacitor 1uF	1.19	1.201	1.22	V
Maximum load current	I_{OUT}	V_{DD}=2.5V	-	-	15	mA
Power on reset voltage threshold value	V_{PWR_LDO}	V_{DD} rising	-	1.001	-	V
		V_{DD} falling	-	0.952	-	
Reference current	I_{REF}	-	820	945	1103	nA
Supply current	I	Full power mode	-	22	-	uA
		Battery mode				
Battery supply current	I_{BAT}	Both modes are active	-	-	0.4	uA

Note:

Full power mode: VBAT pin is not connected. Circuit is powered through VDD pin.

Battery mode: VDD pin supply voltage lower than 0.9V or not connected. Circuit is powered through VBAT pin.