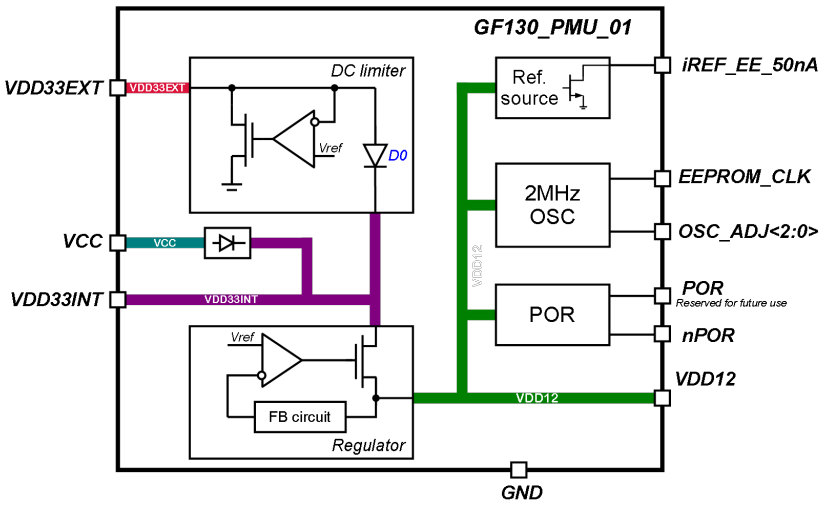
NFC Power Management Unit (1.08 – 1.32 V output voltage, 50 nA output current)

OVERVIEW

130GF_PMU_01 is a Power Management Unit (PMU) block designed to supply embedded integrated circuits with stable and precise voltage, current and clock frequency. IP should derive it's operating power from rectifier or external DC voltage source (Battery assisted operation).

PMU block consists of:

- DC Limiter (shunt);
- Capless low drop out voltage regulator (LDO);
- Reference current source;
- Power-On-Reset module (POR);
- 2 MHz oscillator.



The DC limiter has a built-in diode with a low voltage drop to prevent the discharge of the storage capacity back into the rectifier. The oscillator has frequency control inputs to compensate for process variation.

IP technology: Global Foundries Embedded EEPROM 0.13um.

IP status: pre-silicon verification.

Area: 0.068mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Battery assisted supply voltage	V_{CC}	-	2.4	3.0	3.6	V
Rectified supply voltage	$V_{DD33EXT}$	-	2.2	-	-	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Limiter clamping voltage	V_{LIM}	$I_{DC\_LIM} \leq 50mA$	2.4	3.0	3.6	V
Maximum limiter current	I_{DC_LIM}	-	50	-	-	mA
Voltage regulator output level	V_{DD12}	-	1.08	1.19	1.32	V
Voltage regulator output level standard deviation	Vσ	Mismatch+Process	-	5	-	%
Load capacitance	C_{LOAD}	-	100	250	450	pF
Maximum load current	I_{LOAD}	-	-	-	5	mA
Reference current	I_{REF}	-	45	51	63	nA
POR threshold	V_{PORvth}	-	0.75	0.89	1.02	V
Output clock frequency	F_{OUT}	adj_osc = "000"	-	-	2.1	MHz
		adj_osc = "010"	1.5	2.0	2.8	
		adj_osc = "111"	2.8	-	-	
Voltage regulator current consumption	I_{CC_LDO}	-	2.9	4.5	6.7	uA
Reference source, POR current consumption	$I_{CC\_RS\_POR}$	-	0.26	0.27	0.35	uA
2MHz oscillator current consumption	I_{CC_OSC}	-	0.40	0.55	0.80	uA
Total current consumption*	I_{CC}	$I_{CC} = I_{CC\_LDO} + I_{CC\_RS\_POR} + + I_{CC\_OSC}$	3.56	5.32	7.85	uA
Input logic-high level	V_{IH}	For OSC_ADJ<2:0> inputs	$0.7*V_{DD12}$	-	-	V
Input logic-low level	V_{IL}		-	-	0.3	V

Notes: *Excluding I_{DC_LIM}