Power Management Unit

SPECIFICATION

1 FEATURES

- iHP SG25H4 SiGe BiCMOS 0.25 um
- Bandgap voltage source 1.12 V
- Constant current source
- 500 Hz to 140 kHz frequency generator
- Standby mode
- Portable to other technologies (upon request)

2 APPLICATION

- Battery powered devices
- Core voltage
- Supply voltage sensitive circuits
- Power solutions
- Clocking systems

3 OVERVIEW

PMU IP includes following components: Bandgap reference voltage source, reference current sources and reference frequency generator. Bandgap source forms temperature, power supply and process variations independent voltage.
Reference current sources provide stable output currents which are independent of process/voltage/temperature variations if external resistor is used (CS = “0”) or dependent of process corner and temperature of internal resistor rppd (CS = “1”).
Reference frequency generator could operate in two modes: XTALL mode (OSC_MODE = “0”) and TCXO mode (OSC_MODE = “1”). In XTALL mode external resonator is used, while in TCXO mode external TCXO provides input frequency signal, which is buffered and additionally divided. There are two output frequencies: undivided reference frequency (CLK_REF output) and programmable (OSC_CDiv<7:0>) divided frequency (CLK_REF_DIV). To achieve 50% duty cycle at CLK_REF_DIV output there is additional division-by-two stage embedded in frequency divider, which is turned on by OSC_Div2 = “1”.

4 STRUCTURE

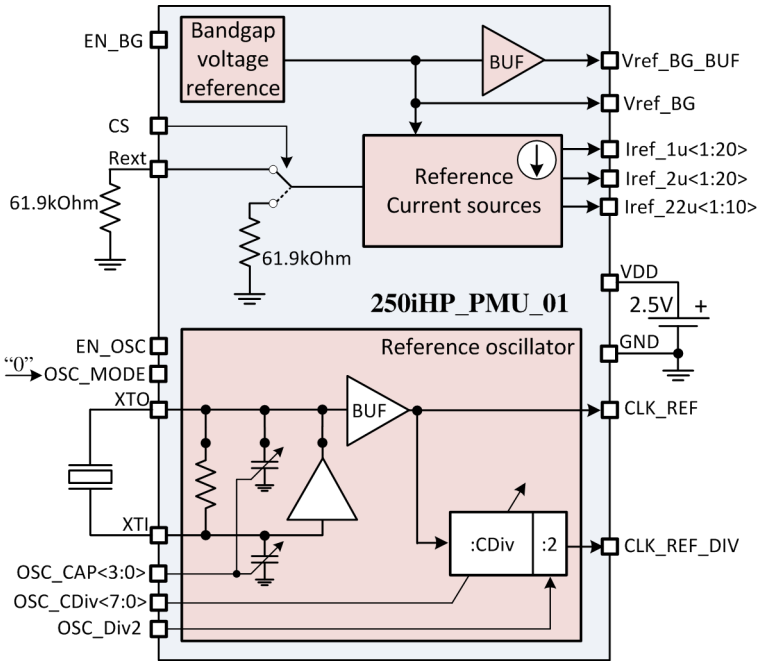

Figure 1: Power Management Unit application diagram with external quartz resonator for frequency generation

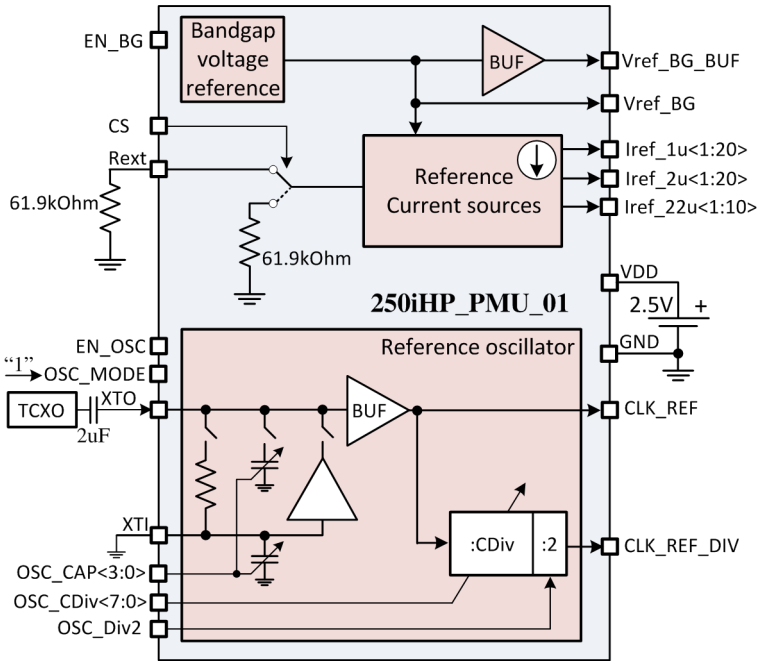

Figure 2: Power Management Unit application diagram with external frequency generator

5 PIN DESCRIPTION

Name	Direction	Description
Bandgap and current sources		
Iref_22u<1:10>	O	22uA output reference current (effluent)
Iref_2u<1:20>	O	2uA output reference current (effluent)
Iref_1u<1:20>	O	1uA output reference current (effluent)
CS	I	Current source mode selection: "0" based on external resistor (default) "1" based on internal resistor
Rext	I	External resistor connection node
EN_BG	I	Bandgap block enable: "0" enabled "1" disabled
Vref_BG_BUF	O	Buffered bandgap reference voltage
Vref_BG	IO	Bandgap reference voltage
Reference frequency generator		
XTO	IO	External quartz resonator 1st connection node; TCXO connection
XTI	IO	External quartz resonator 2nd connection node
EN_OSC	I	Oscillator block enable/disable: "0" enabled "1" disabled
OSC_MODE	I	Oscillator operating mode: "0" with external quartz resonator (default) "1" with external TCXO
OSC_CAP<3:0>	I	Internal oscillator capacitor setting: "000" 9pF "001" 12pF "010" 15pF "011" 18pF (default) … with step of 3pF "111" 30pF
OSC_CDiv<7:0>	I	Output frequency division coefficient: "00000000" 1 "00000001" 1 "00000010" 2 (default) … with step of 1 "11111111" 255
OSC_Div2	I	Additional dividing-by-2 mode for 50% duty cycle: "0" additional dividing disabled "1" additional dividing enabled (default)
CLK_REF	O	Reference frequency output
CLK_REF_DIV	O	Divided reference frequency output
VDD	P	Supply voltage 2.5 V
GND	P	Ground node

Note: I – input, O – output, IO – input/output, P – power line

6 FUNCTIONAL DESCRIPTION

Power management unit (PMU) is used to provide bandgap reference voltage, stable reference currents and reference clock frequency. **EN_BG** = "1" enables bandgap voltage reference source and current sources. To enable reference frequency generator **EN_BG** = "1" and **EN_OSC** = "1". For standby mode **EN_BG** = "0" and **EN_OSC** = "0".

6.1 BANDGAP VOLTAGE SOURCE AND CURRENT SOURCES

EN_BG = "1" enables both bandgap voltage source and current sources. Bandgap reference voltage 1.12V is available at **Vref_BG** output. This output is low power, so no any resistive load is acceptable there. It is supposed that no current will flow into or out of this node. Buffered version of bandgap voltage is available at **Vref_BG_BUF** output, which is capable to drive down to 2 kOhm low resistive load. Please note, that voltage at **Vref_BG_BUF** node could slightly differs from voltage at **Vref_BG** node because of buffer offset due to process variations. Output reference currents are available at corresponding outputs **Iref_22u<1:10>**, **Iref_2u<1:20>** and **Iref_1u<1:20>**. The currents are independent of process/voltage/temperature variations if external resistor is used (**CS** = "0") or dependent of process corner and temperature of internal resistor rppd (**CS** = "1"). External resistor should be connected to **Rext** pin of PMU.

6.2 REFERENCE FREQUENCY GENERATOR

Reference frequency generator could be enabled by **EN_OSC** = "1". It could operate in two modes: XTALL mode (**OSC_MODE** = "0") and TCXO mode (**OSC_MODE** = "1"). In XTALL mode external resonator is used, while in TCXO mode external TCXO provides input frequency signal, which is buffered and additionally divided. In XTALL mode external quartz resonator should be connected to **XTI**, **XTO** pins as it shown in Figure 1. In TCXO mode decoupling 2uF capacitor should be placed between TCXO output and **XTO** pin (see Figure 2); **XTI** pin should be grounded. Reference frequency generator provides two output frequencies: undivided reference frequency (**CLK_REF** output) and programmable (**OSC_CDiv<7:0>**) divided frequency (**CLK_REF_DIV**). In case of **OSC_Div2** = "0" duty cycle of output signal is inversely proportional to frequency division coefficient, which is selected by **OSC_CDiv<7:0>**. To achieve 50% duty cycle at **CLK_REF_DIV** output there is additional division-by-two stage embedded in frequency divider, which is turned on by **OSC_Div2** = "1" (see figure 3).

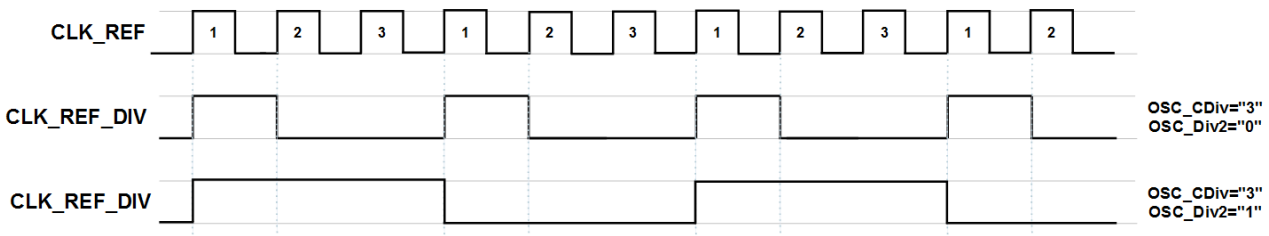

Figure 3: Reference frequency generator transient behavior

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

ADC is designed under iHP 250 nm sg25H4 technology process with following options:

- 3 levels of thin metals and 2 levels of thick are used for routing
- Regular Vt N/P FET
- Rppd resistor is used
- MIM-capacitors are used
- Bipolar devices are used

7.2 PHYSICAL DIMENSIONS

Table 1: Block dimensions

Dimension	Value	Unit
Height	475	um
Width	430	um

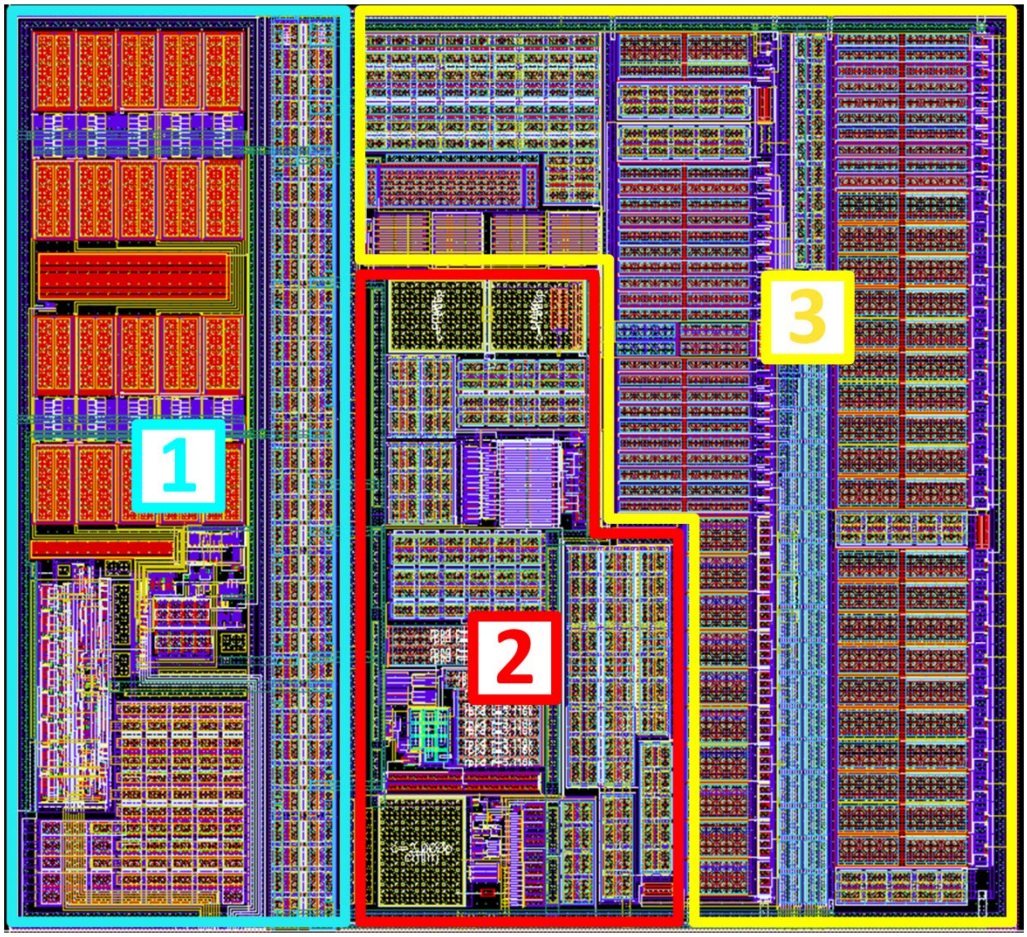

Figure 4: PMU layout

1. XTAL
2. Bandgap
3. Reference course

8 INTEGRATION GUIDELINES

8.1 INPUT AND OUTPUT SIGNALS

It is supposed, that input control pins will be used to change operation mode only and will be unchanged during normal operation.
External resistor's ground (Rext connected resistor) should be shorted to chip ground node.
Output signals rising/falling edges depends on additional capacitance connected to these pin at integration level (see figure 5).

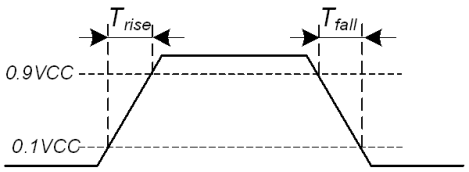

Figure 5: Output signals timing

Load capacity for output signals **CLK_REF** and **CLK_REF_DIV** determinates by following formula:

$$\text{RiseTime}=1.5\ (C_{routing}+55\text{fF}),$$
$$\text{FallTime}=0.55\ (C_{routing}+180\text{fF}),$$

where $C_{routing}$ is routing capacitance.
It is recommended to keep rise and fall times lower than 5ns.

8.2 PLACEMENT AND ROUTING

The following requirements of placement and routing must be satisfied during integration:

1. Power supply (pin VDD) and ground (pin GND) wires should allow flowing of 1 mA DC, 2 mA peak currents and should have total resistance of less than 3 Ohm
2. External capacitance (not less than 10 nF) and internal capacitance should be connected to VDD pin for additional noise filtering. Internal capacitance should be as much as possible
3. Total resistance of wire Rext, which is used to connect external resistor (Rext = 61.9 kOhm), should not exceed 30 Ohm. Internal PAD resistance should not exceed 100 Ohm
4. Filtering capacitance for wire Rext should be 5-10 pF
5. PADs XTI and XTO should be located close to corresponding pins, total resistance at these wires should not exceed 10 Ohm for each wire
6. CLK_REF and CLK_REF_DIV wires are noisy, they should not be placed close to sensitive blocks and wires

PMU is an analog block, which is sensitive to power supply, ground and substrate noise. So, following items below is recommended:

7. For higher reference voltage accuracy it is necessary to make ground and supply wires as short as possible

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ pre-silicon verification
Area _____ 0.2 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{DD} = 2.375 V ÷ 2.625 V, T = 0 °C ÷ +100 °C, unless otherwise noted. Typical values are at V_{DD} = 2.5 V, T = 50 °C.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V_{DD}	-	2.375	2.50	2.625	V
Operating temperature range	T_J	-	0	50	100	ºC
Bandgap reference voltage	V_{REF_BG}	Vref_BG output	1.11	1.12	1.14	V
Bandgap reference voltage temperature dependence	$\Delta_T V_{REF\_BG}$	Vref_BG output	-	-	1	%
Absolute bandgap reference voltage accuracy	ΔV_{REF_BG}	Vref_BG output	-	-	3	%
Reference output currents	I_{REF_1u}	based on external/internal resistor	-	1	-	uA
	I_{REF_2u}			2		
	I_{REF_22u}			22		
Reference voltage load resistance	R_{LOAD}	Buffered	2	-	-	kOhm
		Unbuffered	1	-	-	MOhm
Reference output frequency	F_{REF}	CLK_REF output	32	-	140	kHz
Divided output frequency	F_{REF_DIV}	CLK_REF_DIV output	0.5	32	F_{REF}	kHz
Duty cycle	D	OSC_Div2 = “1”	40	50	60	%
Current consumption	I_{DD}	Active mode: Total	-	TBD	TBD	uA
	I_{STB}	Standby mode	-	0.1	10	nA
Input logic high level	V_{IH}	for digital inputs	V_{DD}-0.25	-	V_{DD}+0.25	V
Input logic low level	V_{IL}		-0.25	-	0.25	V
Max load capacity	C_{load_max}	On Vref_BG output	-	-	5	pF

9.3 TYPICAL OPERATING CHARACTERISTICS

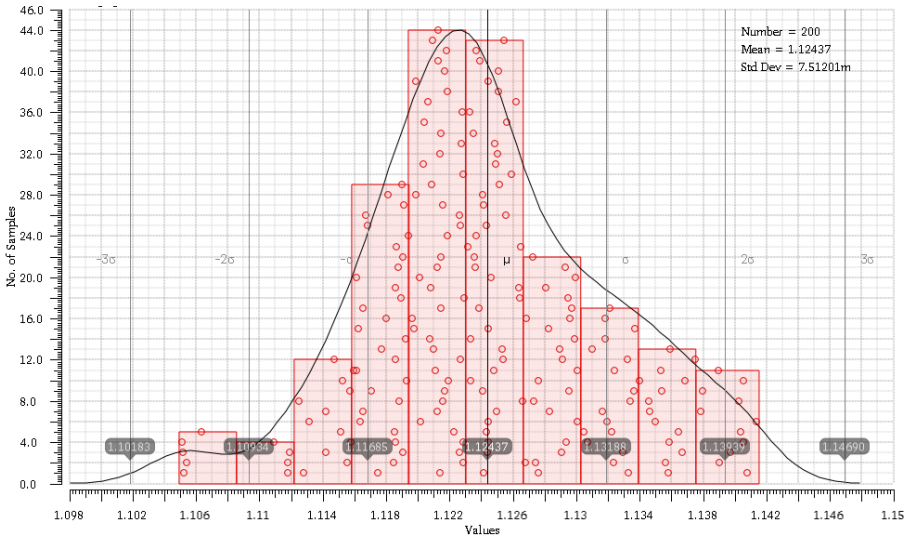

Figure 6: Bandgap Monte Carlo simulation. Vref_BG output. STD = 7.5mV

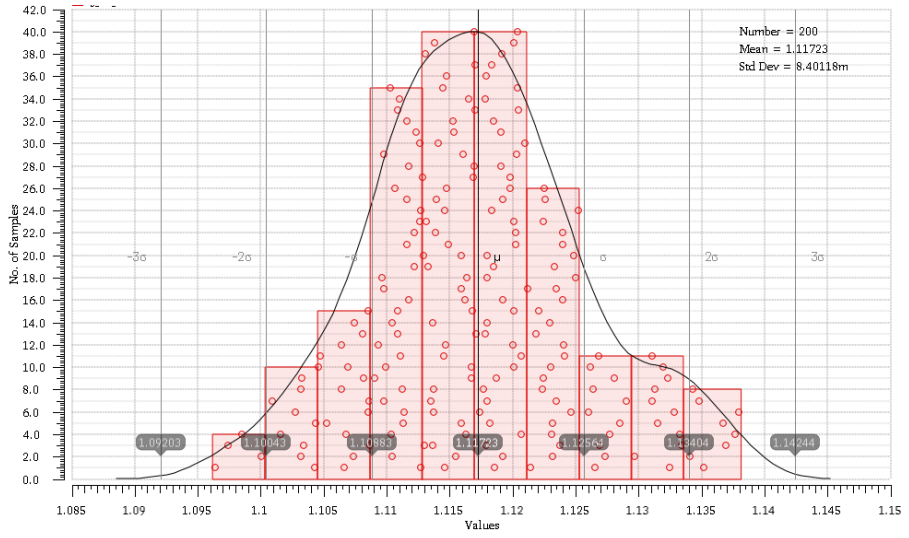

Figure 7: Bandgap buffer Monte Carlo simulation. Vref_BG_BUF output. STD = 8.4mV

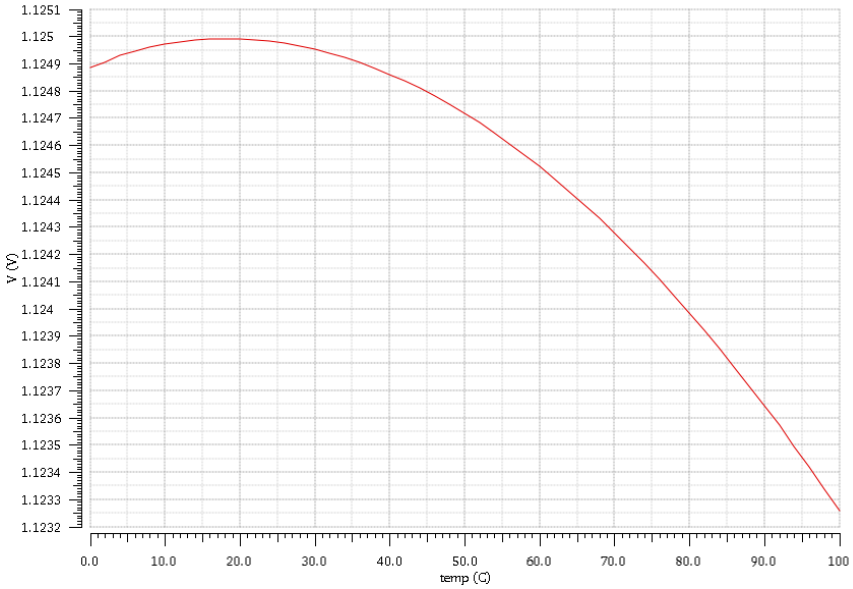

Figure 8: Bandgap voltage vs temperature simulation. Vref_BG output

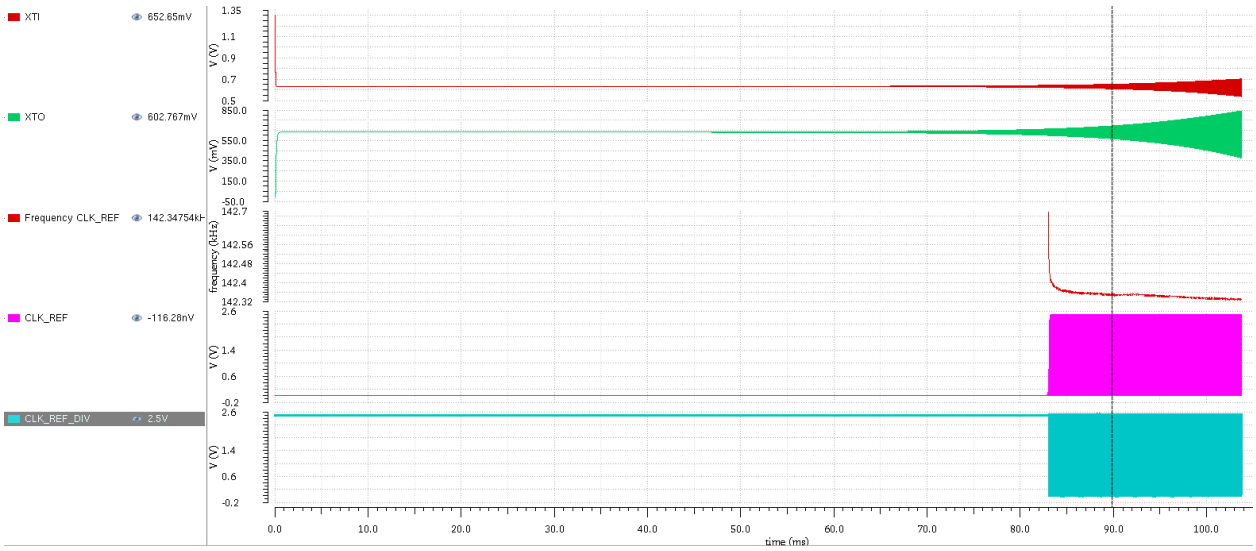

Figure 9: Frequency generator start behavior. XTALL mode

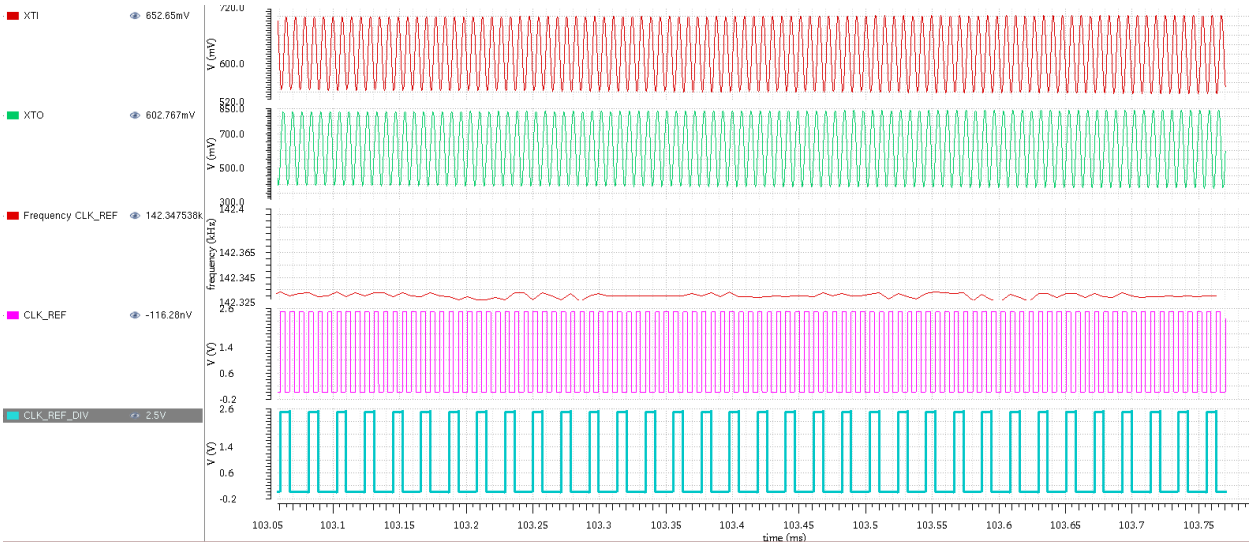

Figure 10: Frequency generator start behavior (detail). XTALL mode

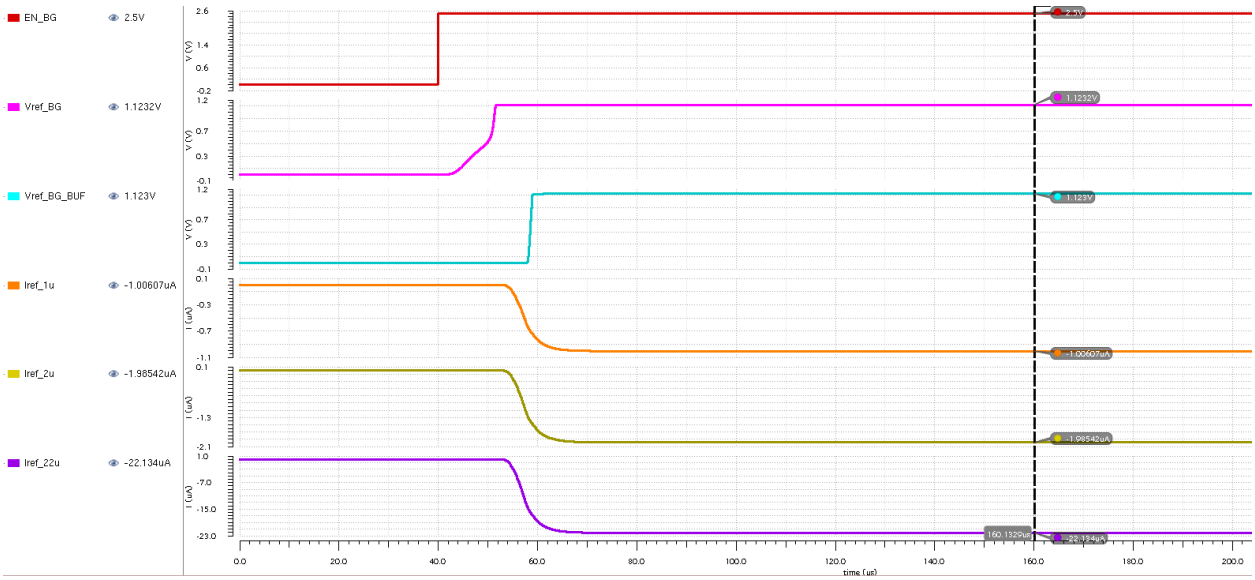

Figure 11: Bandgap reference voltage and reference current sources power on behavior

10 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation