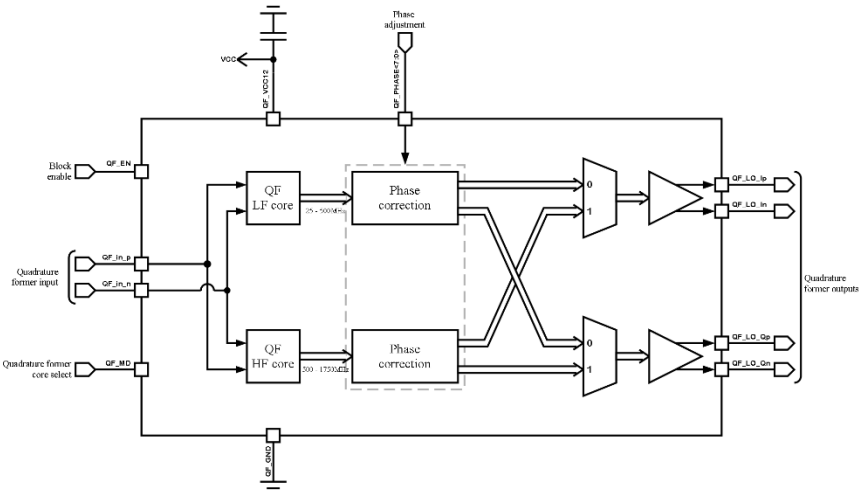
Quadrature former 25-1750MHz

OVERVIEW

The quadrature former block is intended to generate quadrature signal in frequency range 25-1750MHz with phase correction ±4°.The quadrature former core is based on frequency division by 4, implemented on CMOS logic. The block input frequency range 100-7000MHz. The phase correction block uses the dependence of the fronts rise rate of the supply voltage, that in turn affects the phase of the output quadrature signal. The buffers located at the output of the quadrature former, in addition to the output power amplifying, also serve as a junction between the core (frequency divider) and the external blocks.



IP technology: TSMC CMOS 55nm;
IP status: silicon proven;
Area: 0.0348mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Unit
Supply voltage	V_{CC}	-		1.08	1.20	1.32	V
Operating temperature range	T_J	Nominal		-45	+25	+85	°C
Current consumption	I_{CC}	Operating mode	F_{OUT} = 25MHz	-	0.02	-	mA
			F_{OUT} = 500MHz	-	0.5	-	
			F_{OUT} = 1750MHz	-	1.3	-	
		Standby mode		-	0.3	8	µA
		Power-off mode		-	0.1	0.3	nA
QF division ratio	N	-		-	4	-	-
Input frequency range	F_{IN}	mode 1		100	-	2000	MHz
		mode 2		2000	-	7000	
Output frequency range	F_{OUT}	mode 1		25	-	500	MHz
		mode 2		500	-	1750	
Phase adjustment range	Δφ (delta)	F_{OUT} = 125MHz, mode 1		-	0.25	-	degree
		F_{OUT} = 500MHz, mode 1		-	4	-	
		F_{OUT} = 1250MHz, mode 2		-	5	-	
		F_{OUT} = 1750MHz, mode 2		-	16	-	
Phase adjustment accuracy	dφ	F_{OUT} = 125MHz, mode 1		-	0.001	-	degree
		F_{OUT} = 500MHz, mode 1		-	0.016	-	
		F_{OUT} = 1250MHz, mode 2		-	0.02	-	
		F_{OUT} = 1750MHz, mode 2		-	0.07	-	
Input logic-level low	V_{IL}	For digital inputs		0	-	0.1	V
Input logic-level high	V_{IH}			V_{CC}-0.1	-	V_{CC}+0.1	V