GPS/Galileo/GLONASS multisystem single-band receiver

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18 µm
- Single conversion superheterodyne receiver
- Selectable front end modes: IQ GPS/Galileo/GLONASS, IQ GPS/Galileo only, IQ GLONASS only, GPS/Galileo/GLONASS with image-rejection
- Integrated mixer preamplifier with programmable operating current
- Integrated LNA
- Image-rejection mixer
- Integrated IF filter with automatic passband adjustment or external IF filter option
- Independent AGC for each channel with capacitor that set AGC time constant
- Selectable channel output type: differential linear output or digital CMOS output with built-in 2-bit ADC
- Fully integrated frequency synthesizer with internal/external PLL filter
- Clock driver for correlator
- Fully integrated VCO with automatic adjustment system
- PLL lock indicator
- 3-wires serial peripheral interface for status monitoring, mode configuration and parameter adjustment
- «Stand-by» mode with minimum current consumption

2 APPLICATION

- Navigation systems
- Portable receivers
- Mobile communication
- Measuring equipment and etc.

3 OVERVIEW

The NT1019RF is a multisystem receiver intended to perform a simultaneous reception, down conversion, filtering and amplifying of GNSS GPS/Galileo/GLONASS L1-band signals.
IC is fabricated on CMOS SMIC 0.18 µm technology.

4 PAD DESCRIPTION

Pad number	Name	Description
1A	LNA_GND	LNA ground
1B		
2	LNA_OUT	LNA output
3A	LNA_VCC	LNA supply voltage
3B		
DA01	-	Ground
DA02		
4A	MIX_VCC	Mixer supply voltage
4B		
5	MIX_IN	Mixer input
6A	MIX_GND	Mixer ground
6B		
DA03	-	Ground
DA04		
7A	VCO_GND	VCO ground
7B		
8A	VCO_VCC	VCO supply voltage
8B		
DA05	-	Ground
DA06		
9A	DIG_GND	Voltage regulator and serial interface ground
9B		
10A	DIG_VCC	Voltage regulator and serial interface supply voltage
10B		
11	REF_IN	Reference frequency input
12	EN	Serial interface enable
13	DATA	Serial interface input/output data
14	CLK	Serial interface clock
DA07	-	Ground
DA08		
15	CP_OUT	PLL filter output
16A	PLL_VCC	Synthesizer supply voltage
16B		
17A	PLL_GND	Charge pump ground
17B		
DA09	-	Ground
DA10		
18A	MIX_Q_VCC	Q channel LPF supply voltage
18B		
19	MIX_Q_OUTp	Q channel differential mixer output
20	MIX_Q_OUTn	
DA11	-	Ground
21A	MIX_Q_GND	Q channel IFA ground
21B		
DA12	-	Ground
22	IFA_Q_INn	Q channel differential IFA input
23	IFA_Q_INp	

Table 4.1 (continue).

Pad number	Name	Description
DA13	-	Ground
24A	IFA_Q_VCC	Q channel IFA supply voltage
24B		
DA14	-	Ground
25	AGC_Q	Q channel AGC output
26	Q_P/sign	Q channel differential/digital output
27	Q_N/magn	
28A	IFA_Q_GND	Q channel IFA detector ground
28B		
DA15	-	Ground
DA16		
29A	CLK_VCC	ADC and clock driver supply voltage
29B		
30	CLK_2	Clock driver differential output
31	CLK_1	
32A	CLK_GND	ADC and clock driver ground
32B		
DA17	-	Ground
DA18		
33A	IFA_I_GND	I channel IFA detector ground
33B		
34	I_N/magn	I channel differential/digital output
35	I_P/sign	
36	AGC_I	I channel AGC output
DA19	-	Ground
37A	IFA_I_VCC	I channel IFA supply voltage
37B		
DA20	-	Ground
38	IFA_I_INp	I channel differential IFA input
39	IFA_I_INn	
DA21	-	Ground
40A	MIX_I_GND	I channel IFA ground
40B		
DA22	-	Ground
41	MIX_I_OUTn	I channel differential mixer output
42	MIX_I_OUTp	
43A	MIX_I_VCC	I channel LPF supply voltage
43B		
44	REG_CAP	Voltage regulator external filtering capacitor
45	REF_CUR	Reference current source external resistor
DA23	-	Ground
DA24		
46A	LNA_GND	LNA ground
46B		
47	LNA_IN	LNA input
48A	LNA_GND	LNA ground
48B		

5 TYPICAL APPLICATION CIRCUIT

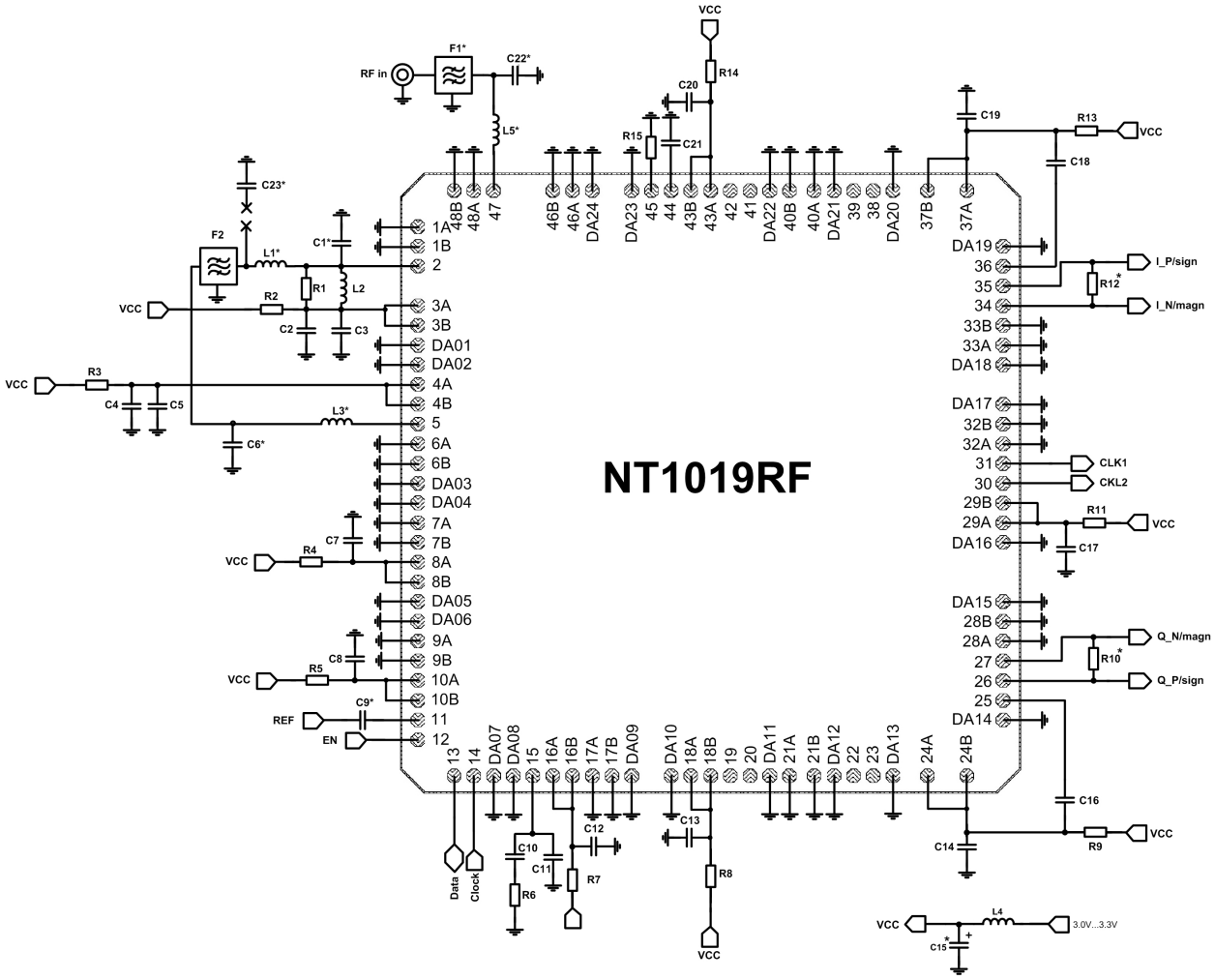

Figure 1: NT1019RF application circuit.

Table 1: External component description.

Component	Nominal value	Tolerance	Notes
C1	2* pF	±5%	Matching network element
C2	0.1 µF	±10%	Supply voltage filter capacitor
C3	220 pF	±10%	Supply voltage filter capacitor
C4	0.1 µF	±10%	Supply voltage filter capacitor
C5	220 pF	±10%	Supply voltage filter capacitor
C6	2* pF	±5%	Matching network element
C7	0.1 µF	±10%	Supply voltage filter capacitor
C8	0.1 µF	±10%	Supply voltage filter capacitor
C9	47* pF	±10%	Blocking capacitor
C10	100 pF	±5%	PLL filter capacitor
C11	10 pF	±5%	PLL filter capacitor
C12	0.1 µF	±10%	Supply voltage filter capacitor
C13	0.1 µF	±10%	Supply voltage filter capacitor
C14	0.1 µF	±10%	Supply voltage filter capacitor
C15	100* µF	±20%	Supply voltage filter capacitor
C16	0.01 µF	±10%	AGC capacitor
C17	0.1 µF	±10%	Supply voltage filter capacitor
C18	0.01 µF	±10%	AGC capacitor
C19	0.1 µF	±10%	Supply voltage filter capacitor
C20	0.1 µF	±10%	Supply voltage filter capacitor
C21	0.01 µF	±10%	Voltage regulator filter capacitor
C22	2* pF	±5%	Matching network element
C23	2* pF	±5%	Matching network element
L1	9.1* nH	±5%	Matching network element
L2	2.7* nH	±5%	Matching network element
L3	6.2* nH	±5%	Matching network element
L6	120 Ω/100 MHz	±20%	Supply voltage filter capacitor
L9	7.5* nH	±5%	Matching network element
R1	700* Ω	±5%	Load resistor
R2	10 Ω	±5%	Supply voltage filter resistor
R3	10 Ω	±5%	Supply voltage filter resistor
R4	10 Ω	±5%	Supply voltage filter resistor
R5	10 Ω	±5%	S Supply voltage filter resistor
R6	20 kΩ	±5%	PLL filter resistor
R7	10 Ω	±5%	Supply voltage filter resistor
R8	10 Ω	±5%	Supply voltage filter resistor
R9	10 Ω	±5%	Supply voltage filter resistor
R10	510* Ω	±5%	Load resistor
R11	10 Ω	±5%	Supply voltage filter resistor
R12	510* Ω	±5%	Load resistor
R13	10 Ω	±5%	Supply voltage filter resistor
R14	10 Ω	±5%	Supply voltage filter resistor
R15	61.9 kΩ	±1%	High precision resistor
F1*	B39162-B9000-C710	-	GPS/Galileo/Glonass L1-band SAW filter
F2	TA0676A	-	GPS/Galileo/Glonass L1-band SAW filter

Note: * – is defined depending on PCB construction and purpose.

6 LAYOUT DESCRIPTION

The chip dimensions are given in the table 2.

Table 2: Block dimensions.

Dimension	Value	Unit
Height	2764.55	µm
Width	2764.55	µm

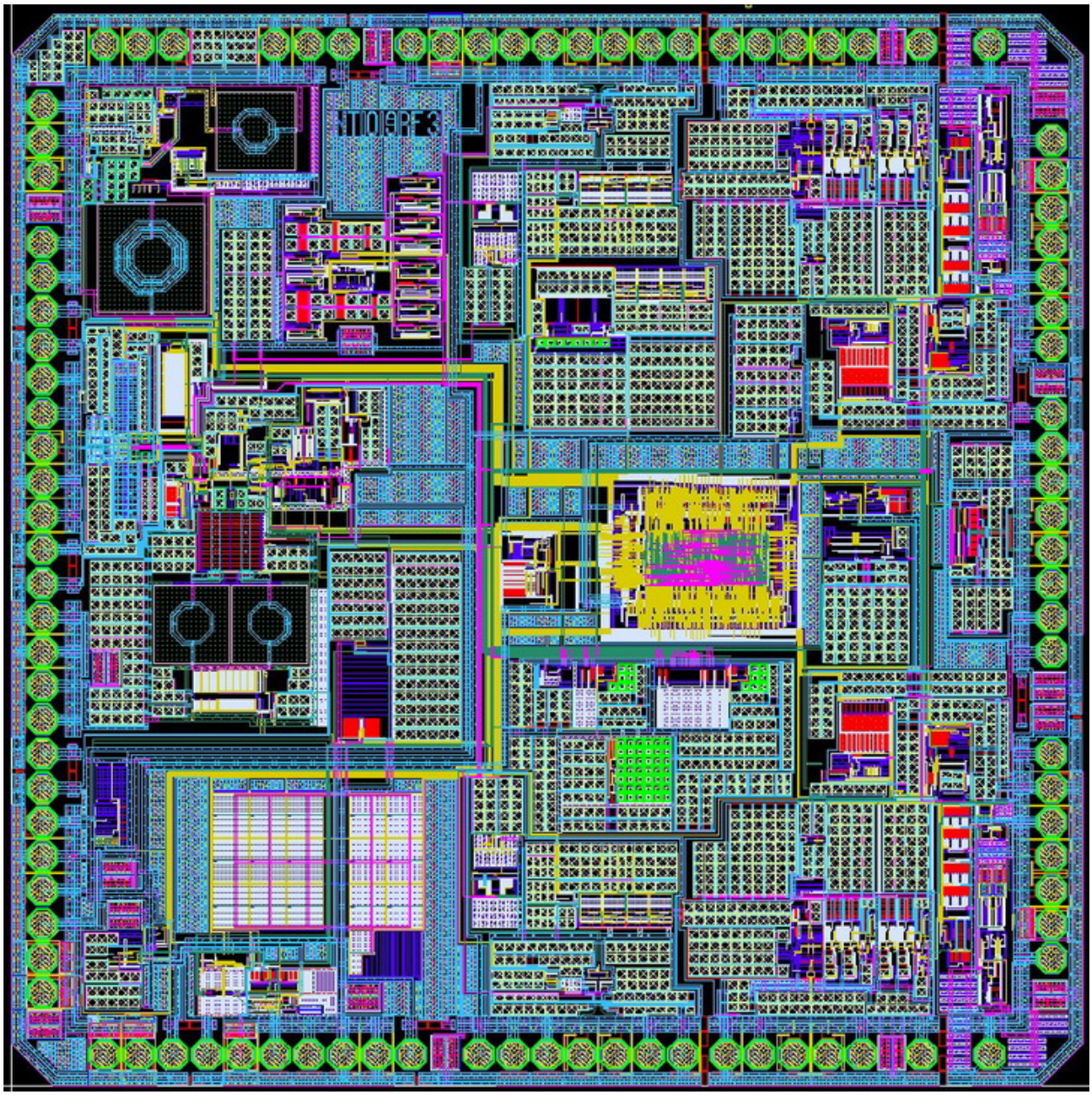

Figure 2:Block layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SMIC CMOS 0.18 µm
Status _____ silicon proven
Area _____ 7.64 mm^2

7.2 DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 3.0 ÷ 3.3 V, T = -40 ÷ +85°C. Typical values are at V_{cc} = 3.15 V, T = +25°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	3.0	3.15	3.3	V
Supply current	I_{cc}	Active mode	-	31.3	32.5	mA
	I_{stb}	Stand-by mode	-	-	1	µA
Output logic-level low (digital outputs)	V_{OH_dig}	For outputs I_P, I_ N, Q_ P, Q_ N. Load current 2 mA	V_{cc}-0.5	V_{cc}-0.2	V_{cc}	V
Output logic-level high (digital outputs)	V_{OL_dig}		0	0.04	0.2	V
Input logic-level low	V_{IL}	-	-0.25	-	0.3	V
Input logic-level high	V_{IH}	-	0.7V_{cc}	-	V_{cc} +0.25	V

7.3 AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 3.0 ÷ 3.3 V, T = -40 ÷ +85°C. Typical values are at V_{cc} = 3.15 V, T = +25°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Overall						
Operating frequency range	F_{IN}	L1 band for GNSS GLONASS	1597.04	-	1606.39	MHz
		L1 band for GNSS GPS and SBAS	1573.13	-	1582.48	
		L1 band for GNSS Galileo	1573.13	-	1582.48	
Noise figure (DSB)	NF	-	-	3.3	4.5	dB
Input VSWR	$VSWR_{IN}$	50 Ω	-	1.1	2.0	dB
Input 1dB compression point	P_{1dB}	-	-58	-55	-	dBm
Overall voltage gain	G_{MAX}	500 Ω	-	80	-	dB
IQ phase accuracy	Δφ	-	-	±0.27	±1.31	degrees
IQ amplitude accuracy	ΔA	-	-	±0.18	±0.21	dB
LNA						
LNA noise figure	NF_{LNA}	-	-	2.9	-	dB
LNA gain	G_{LNA}	-	-	28.5	-	dB
LNA input VSWR	$VSWR_{LNA\_IN}$	50 Ω	-	1.25	-	-
LNA output VSWR	VSWRLNA_OUT	50 Ω	-	1.35	-	-
LNA input 1dB compression point	P1dB_LNA	-	-	-32	-	dBm

Table "AC electrical characteristics" (continue).

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Mixer						
Mixer input VSWR	$VSWR_{Mix\_IN}$	50 Ω	-	16.2	-	-
Mixer output impedance	R_{out_MIX}	Differential	-	1.6	-	Ω
Image rejection	IR	GPS/Galileo	-	500	-	dB
		GLONASS	31	33	-	
LPF&IFA						
Output frequency range	F_{IF}	-	7.28	-	16.64	MHz
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	V_m	500 Ω	-	200/480	-	mV
IFA input impedance	R_{in_IFA}	Differential	-	1	-	kΩ
LPF cut-off frequency	F_{cut_LPF}	-	-	18.1		MHz
AGC range	ΔG	-	50	-	-	dB
ADC						
ADC output signal level	V_{OUT}	-	-	CMOS	-	-
Resolution	R_{ADC}	-	-	2	-	bit
Synthesizer						
PLL dividing ratio	DR_{PLL}	-	-	128	-	-
LO phase noise	PN_{LO}	At 100 kHz offset relative to carrier frequency	-	-89	-	dBc/Hz
		At 1 MHz offset relative to carrier frequency	-	-112	-	
Peak-to-peak voltage at the differential clock outputs	V_{CLK}	4 kΩ	450	-	-	mV
Comparison frequency suppression	S_{FC}	-	80	-	-	dB
Clock frequency	F_{CLK}	-	-	49.68	-	MHz
Reference frequency	F_{REF}	-	-	24.84	-	MHz
LO frequency	F_{LO}	-	-	1589.76	-	MHz

8 DELIVERABLES

IP contents:

- Datasheet
- Layout View (GDSII)
- Evaluation kit based on packaged IC
- Characterization Report
- Behavioral Model
- SPICE netlist (.cdl)
- Integration Support