GLONASS/GPS/Galileo/BeiDou Multisystem Single-band 2-channel Receiver RFIC

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18 µm technology
- Simultaneous GLONASS, GPS, BeiDou and Galileo signals reception
- Single conversion superheterodyne receiver
- Optimized for SiP implementation
- Minimum external components
- 2-input RF MUX with amplifier
- Configurable antenna detector with load and short detection functions
- Stabilized configurable voltage sources for LNA, active antenna and TCXO
- Stabilized separate voltage sources for internal blocks
- Mixer preamplifier with programmable operating current
- Image-rejection quadrature mixer
- Integrated IF filters with band auto-tuning
- Independent IFA AGC for each channel
- Selectable channel output type: differential linear output or digital CMOS output with built-in 2-bit ADC
- Zero offset autocompensation
- Fully integrated synthesizer
- Fully integrated tunable loop filter
- Configurable clock driver for baseband processor
- Fully integrated VCO with automatic adjustment system
- PLL lock indicator
- 4-wire serial peripheral interface for status monitoring, mode configuration and parameter adjustment
- Interrupt signal (diagnostics request) – instant flag showing that IC is in normal functioning mode
- «Stand-by» mode with minimum current consumption
- Different supply schemes (one-voltage, two-voltage)
- 6x6mm QFN40 package option
- 5x5mm QFN32 package option
- 23 external pins in QFN package SiP

2 APPLICATION

- Navigation systems
- Portable receivers
- Mobile communications
- Measuring equipment

3 OVERVIEW

NT1021 is a single-chip dual-channel RF front-end consuming a very low power (47mW typical at 2.1V) and performing a simultaneous reception of both GPS/Galileo/BeiDou and GLONASS signals.

Highly configurable, RFIC can deliver different clock frequencies and provide either analog or digital output using onboard ADC circuits. This, alongside with configurable output CMOS level, makes the circuit compatible with many available baseband ICs.

Integrated stabilized voltage sources for TCXO, external LNA and active antenna alongside with integrated IF and PLL filters make the device easy to use with minimum external components.

RFIC can be delivered in three variants: 6x6mm QFN40 or 5x5mm QFN32 packages, or unpackaged, in dies for SiP implementation.

IC is fabricated on SMIC CMOS 0.18 µm technology.

4 PAD DESCRIPTION

Pad number	Pin Name	Pin Type
1	RF_GND	Ground
2	RF_VCC	Multiplexer-amplifier supply voltage
3	RF_OUT	Multiplexer-amplifier output
4	RF_GND	Ground
5		
6	IFA_GND	
7	MIX_GND	
8	MIX_IN	Mixer input
9	MIX_GND	Ground
10		
11	MIX_VCC	Mixer supply voltage
12	VCO_GND	Ground
13	EXT_RES	Reference resistor output
14	TEST_OUT	Test output
15	VCC33a	External supply voltage
16	REF_IN	Reference oscillator input
17	RO_VCC	Reference oscillator supply voltage
18	SYN_GND	ADC channels, synthesizer and regulators ground
19	DIG_GND	
20	DC_DC_IN	Voltage regulator supply voltage
21	VREF	Reference voltage
22	CLK_OUTN	Clock buffer differential /digital output
23	CLK_OUTP	
24	SCLK	Serial interface clock
25	AOK	Interrupt signal
26	MISO	Serial interface output data
27	MOSI	Serial interface input data
28	EN	Serial interface enable
29	GPSp_m	GPS channel differential/digital output
30	GPSn_s	
31	GLOn_s	GLO channel differential/digital output
32	GLOp_m	
33	IFA_VCC	IFA and IF filters supply voltage
34	IFA_GND	Ground
35	ANT_BIAS	Active antenna supply voltage
36	LNA_BIAS	LNA supply voltage
37	RF_GND	Ground
38		
39	RF_EXT_IN	Multiplexer-amplifier input: signal from LNA
40	RF_GND	Ground
41		
42	RF_INT_IN	Multiplexer-amplifier input: signal from active antenna

5 TYPICAL APPLICATION CIRCUIT

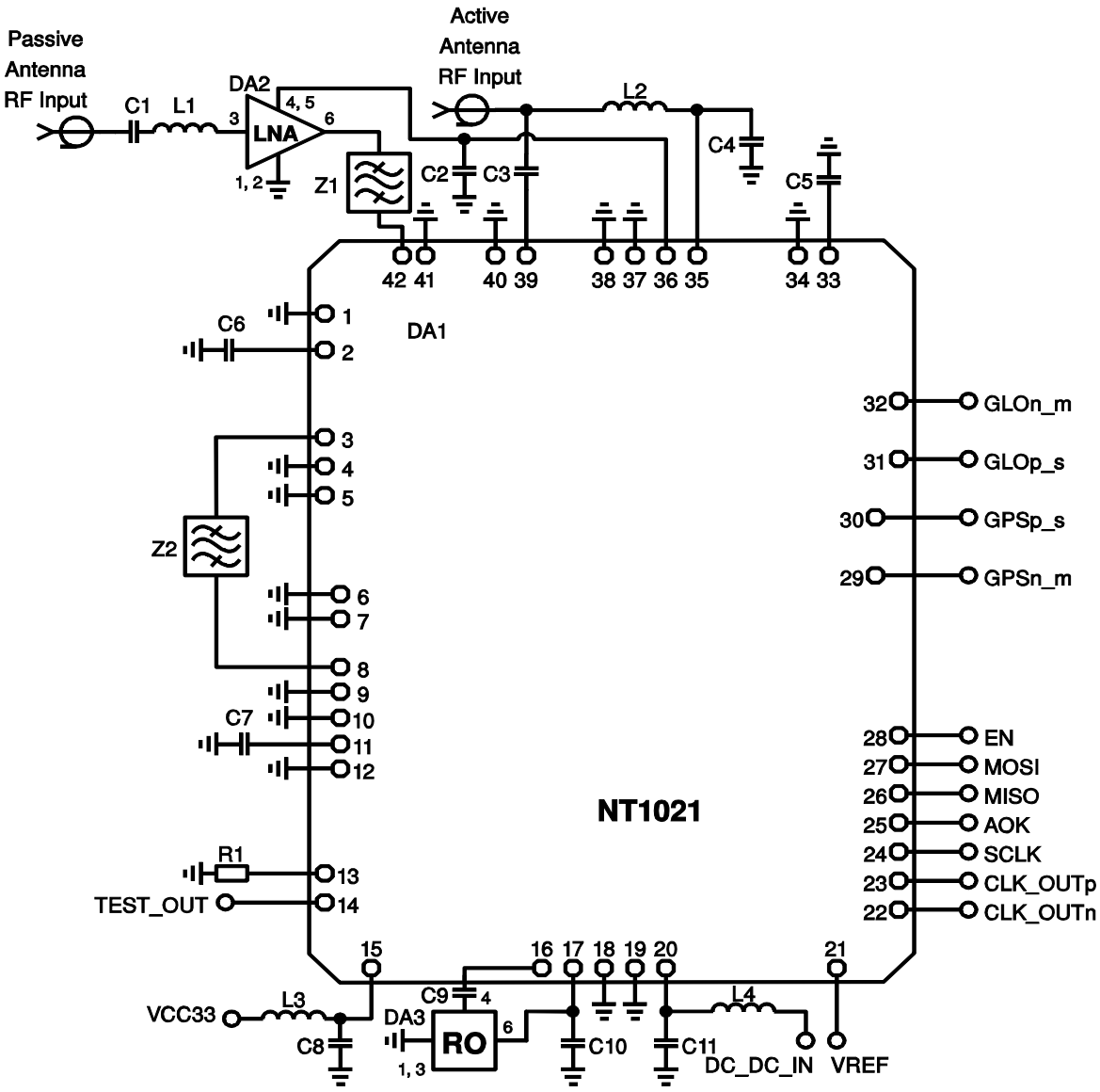

Figure 1: Die application schematic.

Table 1: External component description.

Component	Nominal value	Tolerance	Notes
DA1	-	-	RFIC
DA2	-	-	External LNA
DA3	-	-	TCXO (reference oscillator)
C1	470pF	±5%	LNA input matching capacitor
C2	33nF	±10%	Supply voltage filtering capacitor
C3	470pF	±5%	Active antenna input decoupling capacitor
C4	10nF	±10%	Supply voltage filtering capacitor
C5	0.1µF	±10%	Supply voltage filtering capacitor
C6	0.1µF	±10%	Supply voltage filtering capacitor
C7	0.1µF	±10%	Supply voltage filtering capacitor
C8	1.0µF	±10%	Supply voltage filtering capacitor
C9	33pF	±10%	RO signal input decoupling capacitor
C10	0.1µF	±10%	Supply voltage filtering capacitor
C11	0.1µF	±10%	Supply voltage filtering capacitor
L1	6.8nH	±5%	LNA input matching inductor
L2	56nH	±5%	Active antenna input decoupling inductor
L3	4.7µH	±10%	Supply voltage filtering inductor
L4	4.7µH	±10%	Supply voltage filtering inductor
R1	61.9kΩ	±1%	Reference high precision resistor
Z1*	-	-	RF SAW filter for L1 GPS/Galileo/GLONASS signal (special part for BeiDou support required)
Z2	-	-	RF SAW filter for L1 GPS/Galileo/GLONASS signal (special part for BeiDou support required)

* - defined depending on PCB construction and purpose

6 LAYOUT DESCRIPTION

The chip dimensions are given in the table 2.

Table 2: Chip dimensions.

Dimension	Value	Unit
Height	3036.1	µm
Width	2275.7	µm

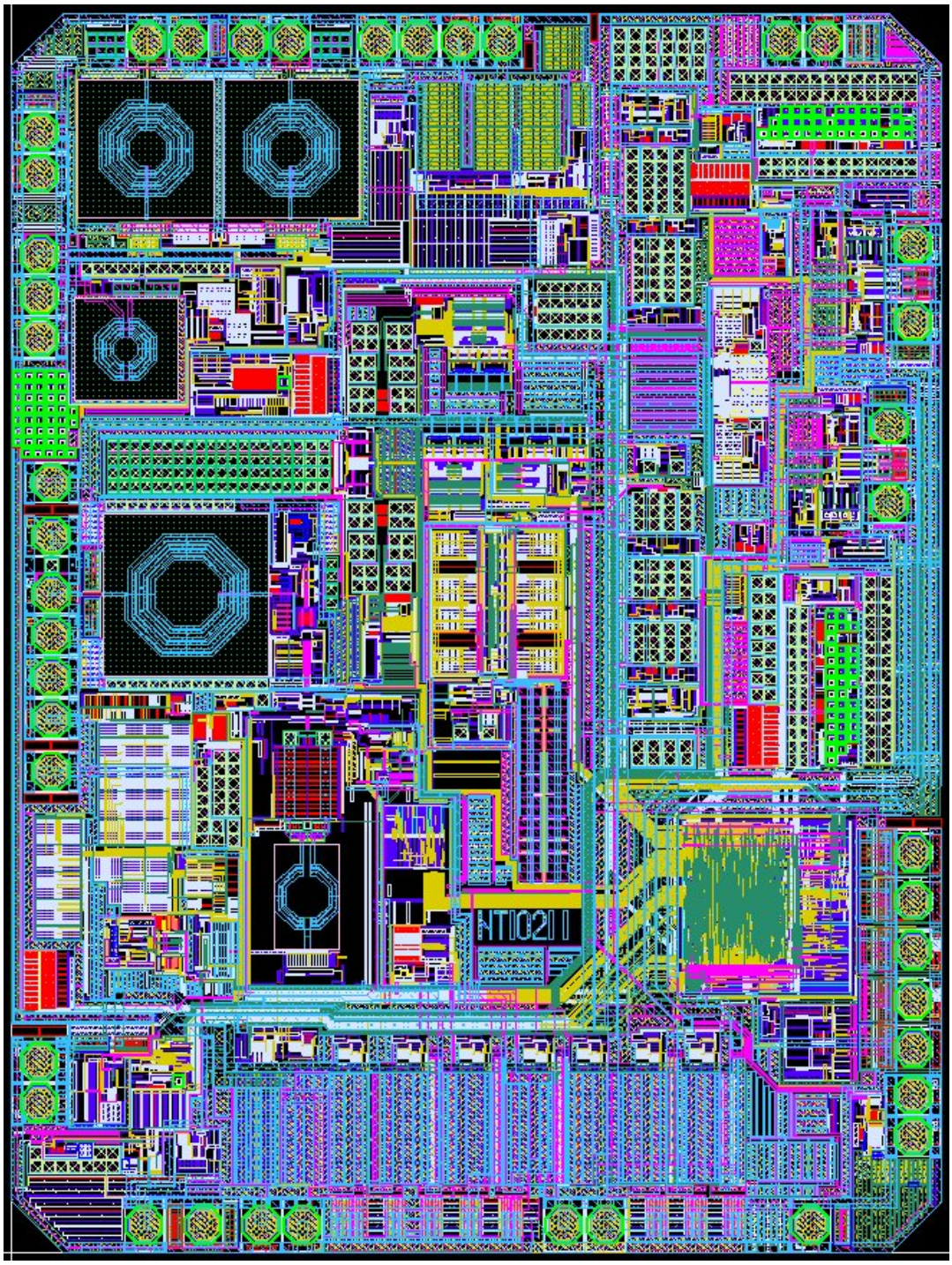

Figure 2: Chip layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SMIC CMOS 0.18 µm
Status _____ silicon proven
Area _____ 6.9 mm^2

7.2 DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc}=2.7 ÷ 3.6 V, V_{dcdc}=+2.0 ÷ +3.6 V and T =-40 ÷ +85°C, unless otherwise specified; Typical values at V_{cc} = 3.3V, V_{dcdc} = +2.1 V and T = +25°C.

Parameter	Name	Conditions	Value			Units
			Min	Typ	Max	
Supply voltage at VCC33a input	V_{cc}	-	2.7	3.3	3.6	V
Supply voltage at DC_DC_IN input	V_{dcdc}	-	2.0	2.1	3.6	V
Current consumption (VCC33a)	I_{cc}	Analog outputs mode	-	0.9	1.1	mA
		Built-in ADC mode	-	0.9	1.1	
Current consumption (DC_DC_IN)	I_{dcdc}	Analog outputs mode	-	21.5	27.0	mA
		Built-in ADC mode	-	21.5	28.0	
Stand-by current	I_{stby}	-	-	0.1	2.6	µA
High CMOS input level	V_{hi}	-	1.5	-	V_{cc}+0.25	V
Low CMOS input level	V_{lo}	-	-0.25	-	0.4	V

7.3 AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc}=2.7 ÷ 3.6 V, V_{dcdc}=+2.0 ÷ +3.6 V and T =-40 ÷ +85°C, unless otherwise specified; Typical values at V_{cc} = 3.3V, V_{dcdc} = +2.1 V and T = +25°C.

Parameter	Name	Conditions	Value			Units
			Min	Typ	Max	
General parameters						
Operating frequencies range	F_{in}	-	1559.05	-	1606.39	MHz
Output frequencies range of GLONASS/GPS/Galileo	F_{OUT_GLO}	-	7.2805	-	16.6370	MHz
	F_{OUT_GPS}	LPF mode	10.2480	-	18.4320	
		Galileo BPF	12.2940	-	16.3860	
		GPS BPF	13.3170	-	15.3630	
		BeiDou BPF	-	-	-	
Output frequencies range of GLONASS/GPS/Galileo/BeiDou	F_{OUT_GLO2}	GLONASS BPF	14.1400	-	23.7025	MHz
	F_{OUT_BeiDou}	LPF mode	5.8940	-	24.3080	
Noise figure (DSB)	NF	-	-	9.0	-	dB
Noise figure with external LNA	NF_{LNA}	MAX2659 is used	-	1.6	-	dB
1dB compression point	P1dB	-	-	-45	-	dBm
Maximum gain	Gmax	-	-	60	-	dB
Multiplexer-amplifier						
MUX-amp input matching	$VSWR_{MA\_IN}$	-	-	1.1	2.0	-
MUX-amp output matching	$VSWR_{MA\_OUT}$	-	-	1.6	2.0	-
MUX-amp input 1dB compression point	P1dB_MA	-	-	-12.6	-	dBm
Gain	GMA	-	-	7.1	-	dB
Noise figure	NFMA	-	-	4.2	-	dB

Table “AC Electrical Characteristics” (continue)

Parameter	Name	Conditions	Value			Units
			Min	Typ	Max	
Mixer and polyphase filter						
Mixer input matching	$VSWR_{MIX\_IN}$	-	-	1.4	2.0	-
Image rejection	IR	-	-	30	-	dB
Synthesizer						
Reference frequency	F_{REF}	-	5	24.84	50	MHz
LO frequency	F_{LO}	-	-	1589.76	-	MHz
PFD frequency	F_{FC}	-	-	24.84	-	MHz
LO phase noise	PN_{LO}	at 10kHz offset	-	-85	-	dBc
		at 100kHz offset	-	-88.34	-	
		at 1MHz offset	-	-115.79	-	
Reference frequency spur suppression	S_{FC}	-	65	90	-	dB
LPF and IFA						
Output frequency range	F_{OUT}	-	7.28	-	16.63	MHz
Sine/noise signal amplitude on linear differential outputs	V_M	Analog outputs mode	180/430	200/480	220/530	mV diff p-p
Linear output DC offset	V_{DC_OUT}	Analog outputs mode	1.15	1.4	1.75	V
Logical one level in ADC mode	V_{OUT_HI}	Built-in ADC mode	1.2	1.8*	1.8	V
AGC works using	-	Analog outputs mode	Output signal RMS			-
		Built-in ADC mode	Magnitude signal filling			
AGC range	ΔG_{AGC}	-	50	57	-	dB
Clock frequency buffer						
Clock signal type	-	Analog outputs mode	Differential			-
		Built-in ADC mode	CMOS meander			
Clock frequency GPS/Galileo/GLONASS	F_{CLK}	-	24.84	49.68	49.68	MHz
Clock frequency GPS/Galileo/GLONASS/BeiDou	F_{CLK_BeiDou}	-	24.74	49.48	49.48	MHz
Output clock signal amplitude	V_{CLK}	Analog outputs mode	0.4	0.7	-	Vdiff p-p
Output clock signal DC offset	V_{DC_CLK}	Analog outputs mode	1.43	1.6	1.79	V
Logical one level in CMOS mode	V_{CLK_HI}	Built-in ADC mode	1.2	1.8*	1.8	V

* - is configurable through serial interface

8 TYPICAL OPERATING CHARACTERISTICS

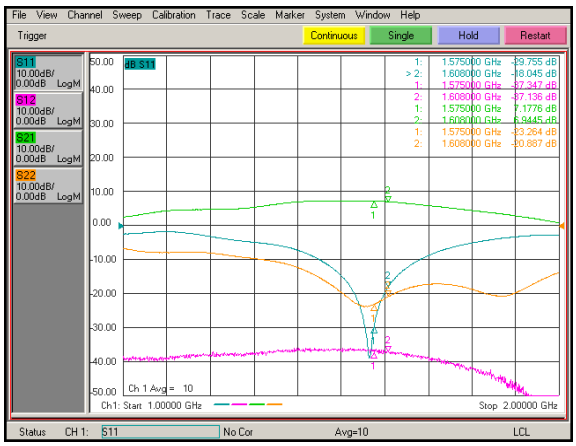

Figure 3: Multiplexer matching and gain.

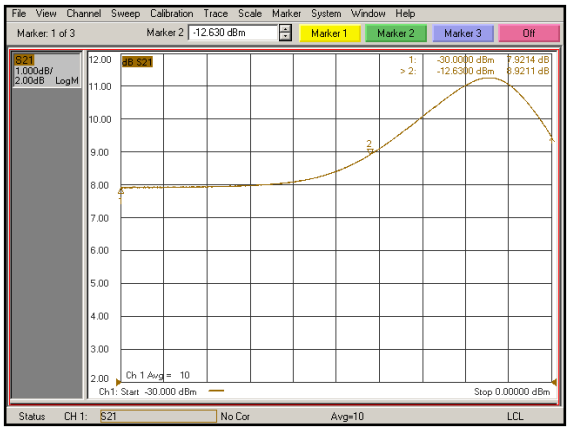

Figure 4: Multiplexer gain vs. input power.

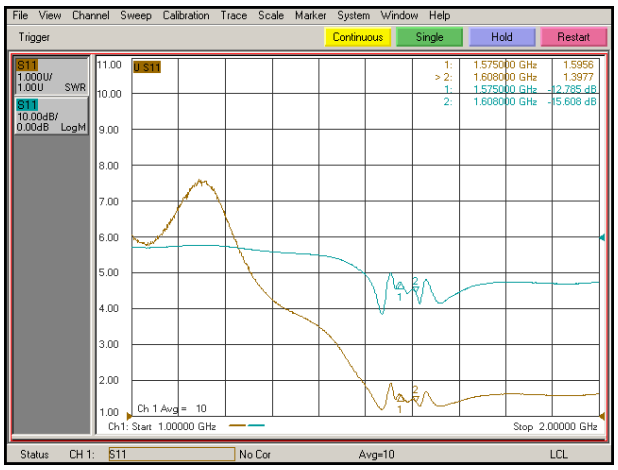

Figure 5: External LNA input matching.

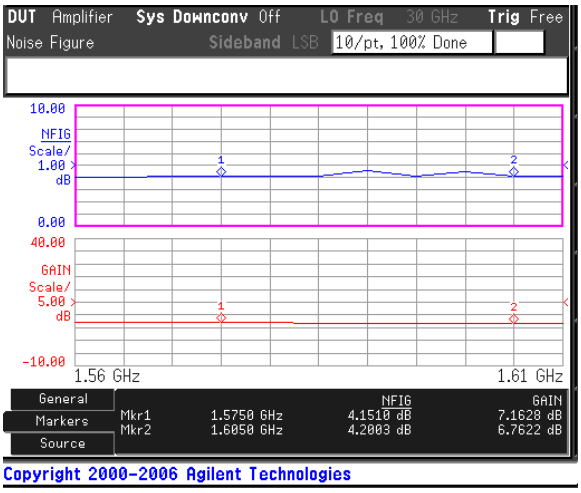

Figure 6: Multiplexer gain and noise figure.

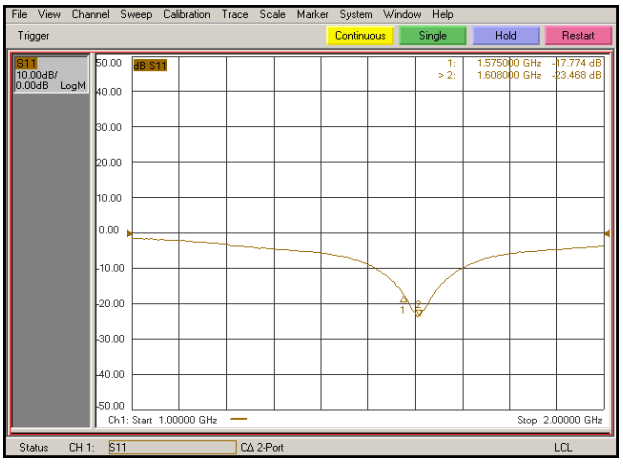

Figure 7: Mixer input matching.

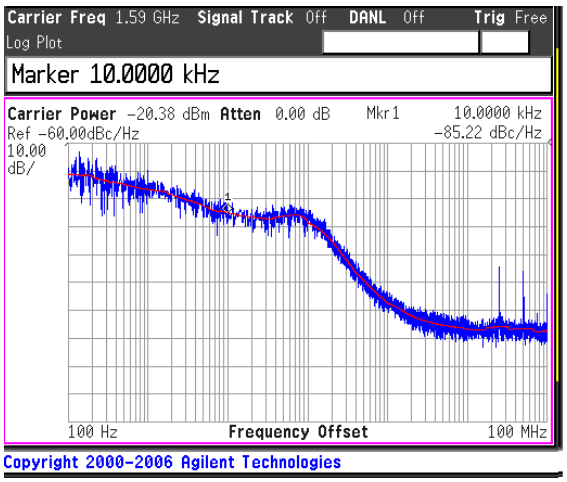

Figure 8: Local-oscillator phase noise.

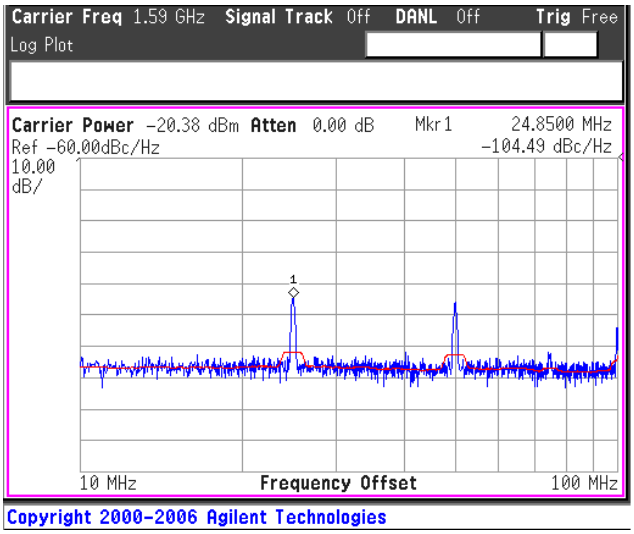

Figure 9: Local-oscillator phase noise at range of 10…100MHz.

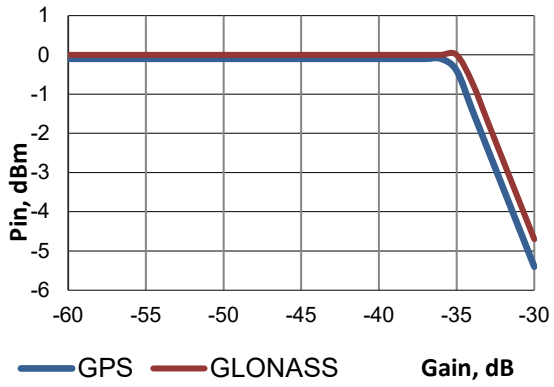

Figure 10: RFIC gain change vs. input power, mixer input.

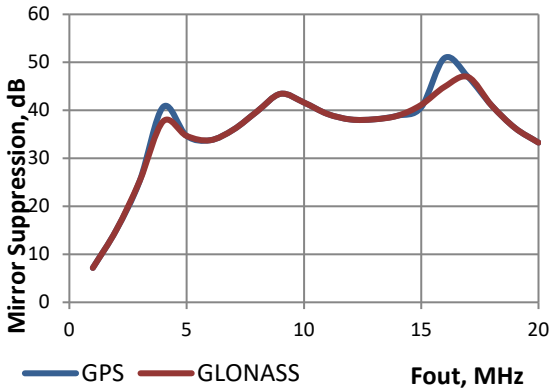

Figure 11: GPS channel image rejection.

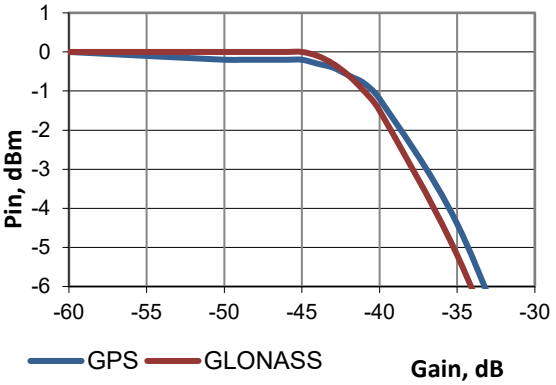

Figure 12: RFIC gain change vs. input power, active antenna input.

9 DELIVERABLES

IP contents:

- Datasheet
- Layout View (GDSII)
- Evaluation kit based on packaged IC
- Characterization Report
- Behavioral Model
- SPICE netlist (.cdl)
- Integration Support