Bandgap voltage reference

SPECIFICATION

1 FEATURES

- Global Foundries CMOS 55 nm
- Output voltage reference 0.4 V
- Output currents reference 250 nA
- Low current consumption
- Small area
- Temperature-compensated voltage in a wide temperature range
- Portable to other technologies (upon request)

2 APPLICATIONS

- Voltage regulators
- Comparison and detection systems
- System-on-chip for different purposes
- Measurement and calibration systems
- Technological research of microelectronic components
- Navigation systems

3 OVERVIEW

The bandgap voltage reference generates temperature-compensated voltage due to mutual compensation of temperature dependence of bipolar diodes and resistors. It is a simple to configure and operate block, combining good parameters accuracy, small area and low current consumption. The block consists of bandgap, buffer and current sources. The bandgap produces on pin out voltage level around 0.4 V, which adjusted by a trimming codes. The buffer repeats the value of the reference voltage. Signals, en_vbgbuf and en_testmode, control the buffer. Each current source delivers a current of 250 nA.
The block is designed on Global Foundries CMOS 55 nm technology.

4 FUNCTIONAL DESCRIPTION

4.1 PINS FOR ENABLING AND DISABLING BLOCK

Input signal en should be set to logical “1” or logical “0”. The high level of the signal turns on block and a low level signal disables it. If input signal en is set to logical “0”, the bandgap voltage reference is switched off independently of the signals en_testmode and en_vbgbuf. Behavior of outputs signals during switching on and off block is shown at Figure 1.

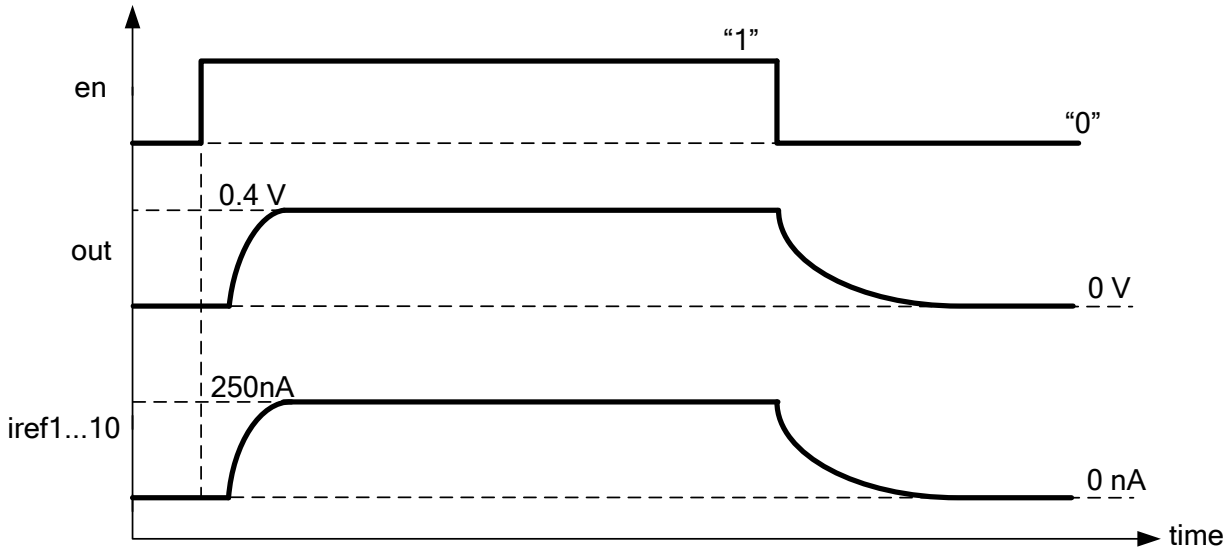

Figure 1: Timing diagram of switching on and off signals out and iref1…10

Behavior of output signal out_buf during switching on and off signals en_testmode and en_vbgbuf shown at Figure 2.

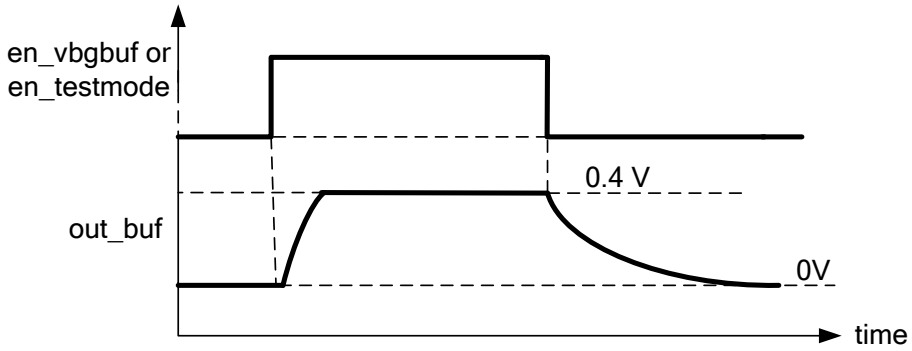

Figure 2: Timing diagram of switching on and off signal out_buf

4.2 PINS FOR TRIMMING THE OUTPUT VOLTAGE

Dependence of the output signal out from trimming code is shown at Figure 3. The output signal out increases linearly with the code as it is shown in table section 6.

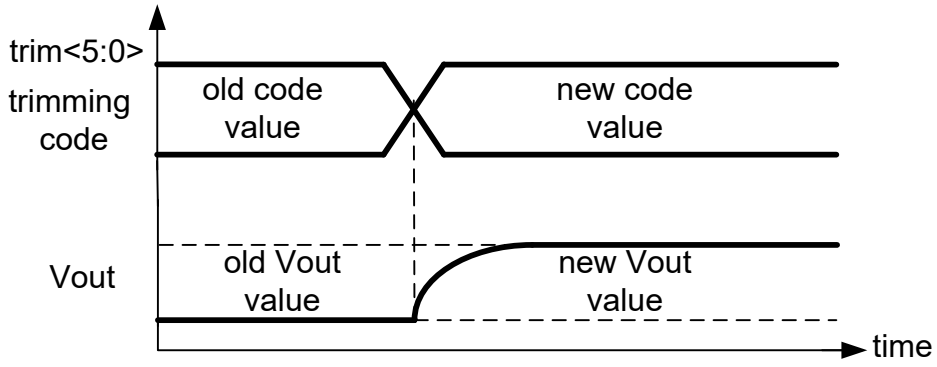

Figure 3: Timing diagram output signal out vs trimming code

4.3 PINS FOR OUTPUT SIGNALS

Pins for output signals are bandgap output pin out and buffer output pin out_buf.
Output pin out assumes a capacitive load up to 2 pF. The load is connected between the output and ground. Resistive load is not permitted.
Output pin out_buf assumes a capacitive load up to 100 pF and DC load from 0 to 200uA. By increasing the load capacitance will increase the settling time. If exceed the current load, the correct voltage is not guaranteed.

5 STRUCTURE

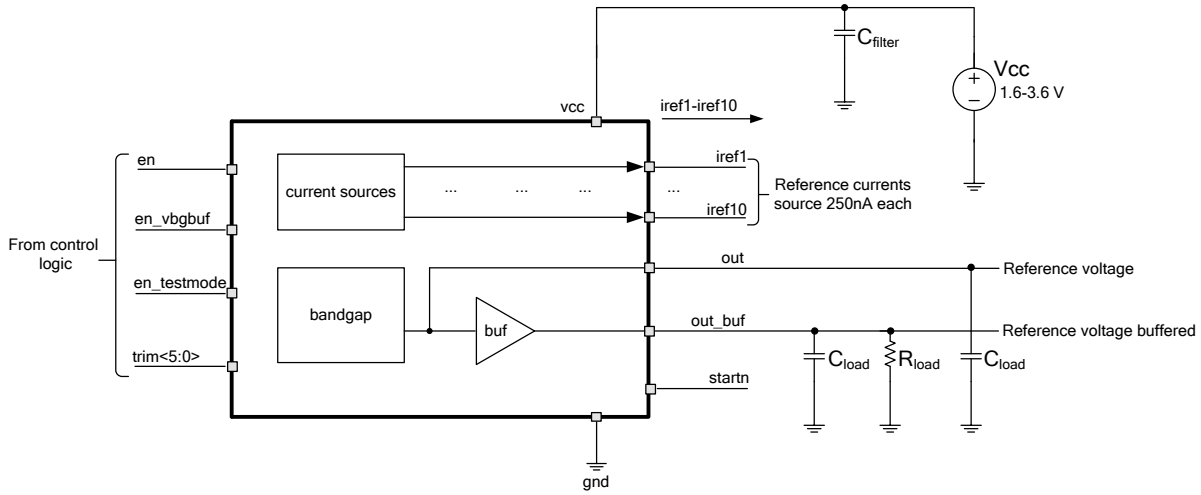

Figure 4: Bandgap voltage reference structure and application diagram

6 PIN DESCRIPTION

Name	Direction	Description
en	I	Bandgap enable: "0" disabled "1" enabled
en_testmode	I	Impedance for buffer output (see table 1): "0" high impedance "1" low impedance
en_vbgbuf	I	Bandgap buffer enable: "0" disabled "1" enabled
trim<5:0>	I	Bandgap trimming value: "000000" 0.3678 V … ~ step 1.04 mV "100000" 0.4011 V … ~ step 1.04 mV "111111" 0.4331 V
out	IO	Bandgap output
out_buf	IO	Bandgap buffer output
iref1…iref10	IO	Reference currents, 250 nA each pin, source mode
startn	O	Status indicator
vcc	IO	Supply voltage
gnd	IO	Ground

Note: * I – input, O – output

Pins en_testmode and en_vbgbuf control the modes of the buffer, see the table below.

Table 1: True table for buffer modes

en_vbgbuf	en_testmode	Mode buffer
"0"	"0"	disabled
"1"	"0"	enabled, high impedance for buffer output
"X"	"1"	enabled, low impedance for buffer output

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

Bandgap voltage reference is designed under Global Foundries CMOS 55 nm technology process with following options:

- 4_02_00_00_LB option
- 2 metal levels of 1x (thin) width are used for routing
- Thick-oxide native (DG) NFET
- Thick-oxide I/O NFET and PFET (3.3V)
- Vertical PNP bipolar transistor
- P+ polysilicon OP resistor
- APMOM capacitor

7.2 PHYSICAL DIMENTIONS

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	97	um
Width	360	um

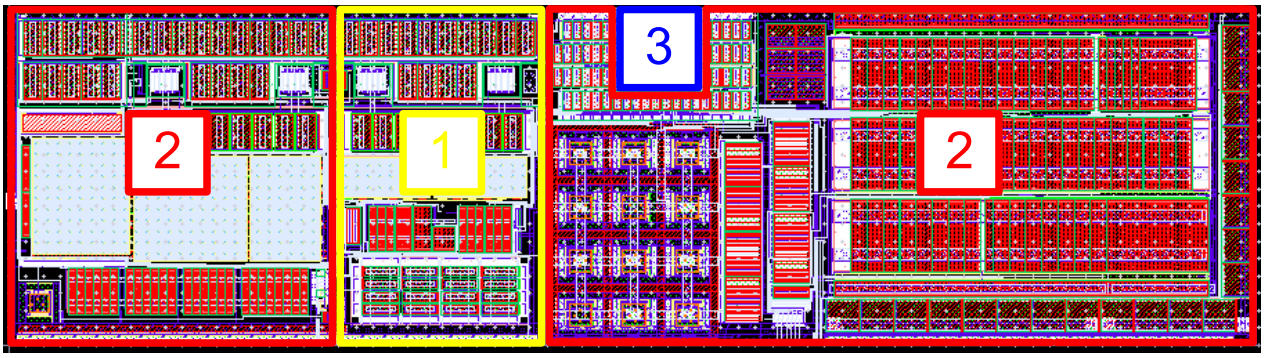

Figure 5: Bandgap voltage reference layout

1. Buffer
2. Bandgap
3. Current sources

8 INTEGRATION GUIDELINES

8.1 INPUT AND OUTPUT SIGNALS

Digital input signals, therefore not subject to special requirements.
Capacitance of pin en is 41 fF.
Capacitance of pin en_testmode is 9 fF.
Capacitances of pins en_vbgbuf, trim<5:0> is 5 fF.
Capacitance of pin startn is 7 fF.

8.2 PLACEMENT AND ROUTING

Bandgap voltage reference is an analog block, which output voltage and current are guaranteed in the range from the table of electrical characteristics, but is necessary provide a small noise on power and ground circuits. So, the following recommendations are given:

1. Bandgap voltage reference layout can be rotated and flipped in axis X and Y
2. IP should be used in the 3.3 voltage domain
3. Power supply (pin vcc) and ground (pin gnd) wires should allow flowing of 0.1 mA DC, 0.5 mA peak currents and should have resistance of less than 10 Ohm between pins and pads
4. For higher reference voltage accuracy is necessary wires for supply and ground to make shorter as possible
5. External capacitance (not less than 0.5 nF) and internal capacitance should be connected to vcc pin for additional noise filtering. Internal capacitance should be added as much as possible
6. No routing is allowed over the block in layers M1—M2

Other pins, not described here, have no special routing guidelines.

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology _____ Global Foundries CMOS 55 nm
Status _____ silicon proven
Area _____ 0.035 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for Vcc = 1.6 ÷ 3.6 V and T = -40 ÷ 85 °C. Typical values are at Vcc = 2.5 V and T = 27 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Supply voltage	Vcc	-	1.6	2.5	3.6	V
Operating temperature range	T	-	-40	27	85	°C
Output voltage	V_{out}	-	-	0.4	-	V
Output voltage accuracy		Non-trimmed	-	4	-	%
		Trimmed	-	1	-	
Trimming range of output voltage		-	-	±5	-	%
Output reference current	I_{ref}	-	200	250	300	nA
Current Consumption	I_{cc}	Buffer disabled	-	10	-	uA
	I_{cc1}	Buffer enabled, high impedance for buffer output	-	13.5	-	
	I_{cc2}	Buffer enabled, low impedance for buffer output	-	200	-	
Input logic-level low	V_{IL}	For digital signals	0	-	0.3*Vcc	V
Input logic-level high	V_{IH}		0.7*Vcc	-	Vcc	

10 TYPICAL CHARACTERISTICS

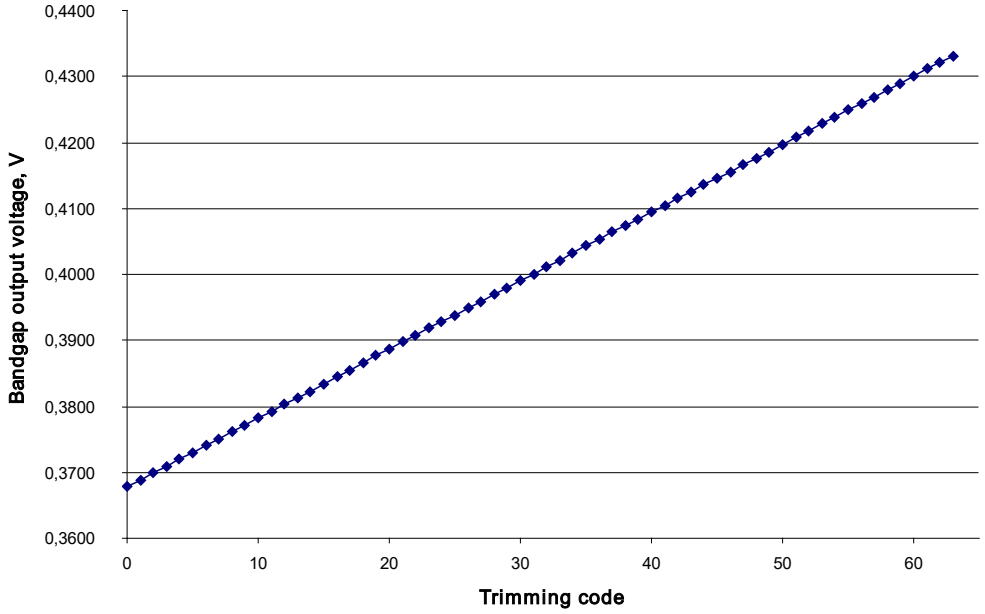

Figure 6: Bandgap output voltage vs trimming code

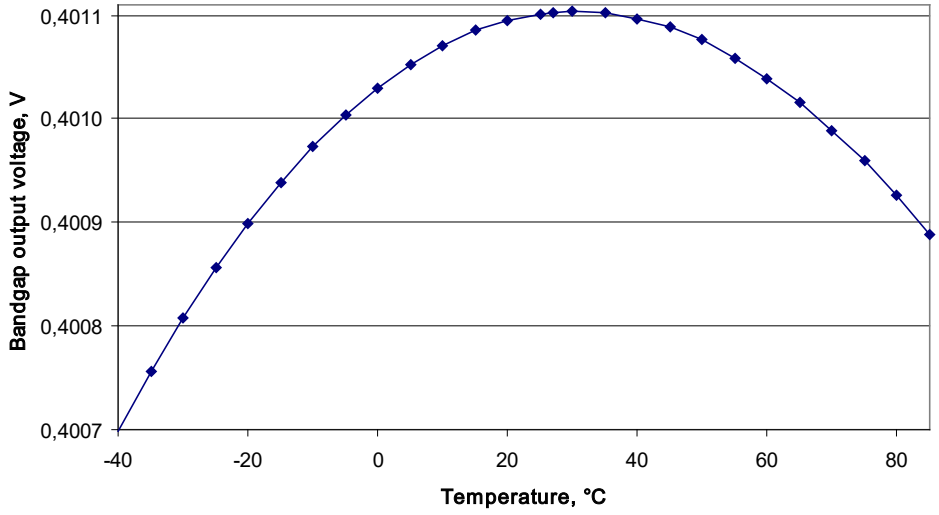

Figure 7: Bandgap output voltage vs temperature

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

12 REVISION HISTORY

From version 1:

- Section 6 “Pin description” updated:
  - Description “trim<5:0>” was changed
- Subsection 7.2 “Physical dimensions”. Table 1 updated
- Subsection 8.1 “Input and output signals” updated
- Subsection 9.2 “Electrical characteristics” updated:
  - Parameters “Input logic-level high” and “Input logic-level low” were added
- Section 10 “Typical characteristics” updated