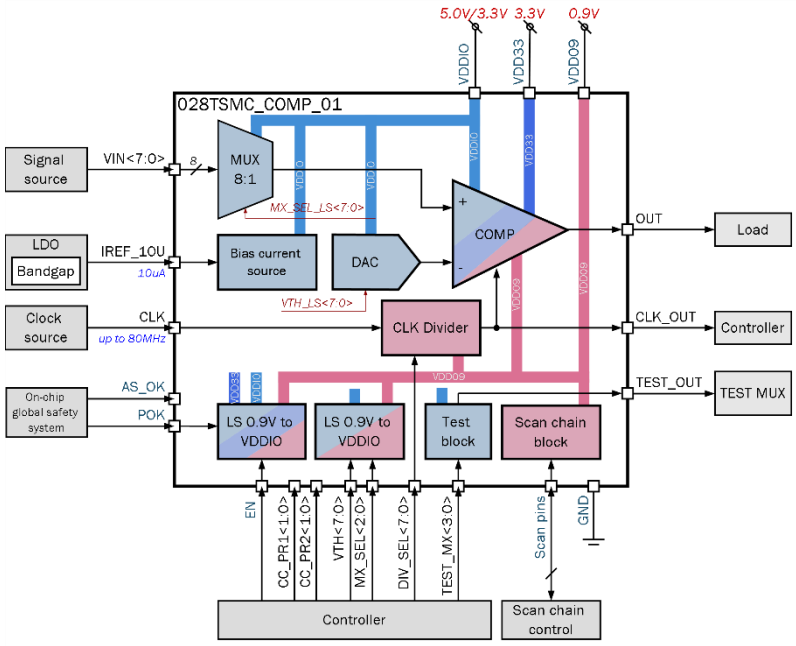
8-channel 8-bit voltage comparator

OVERVIEW

028TSMC_COMP_01 is a comparator that compares a reference voltage to an analog input voltage and contains 8 input channels with a programmable threshold, implemented using 8-bit digital-to-analog converter (DAC).
Conversion time is 25ns in worst case.
The block consists of input multiplexer 8:1, 8-bit DAC and 1-channel comparator.
The Comparator operates from analog VDDIO 3.3V/5.0V, VDD33 3.3V and digital voltage VDD09 0.9V. Bias currents should be delivered from an external source.
IP technology: TSMC 28nm eFlash.
IP status: pre-silicon verification.
Silicon area: 0.06mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Analog supply voltage	V_{DDIO}	Option 5V		4.5	5.0	5.5	V
		Option 3.3V		2.97	3.3	3.63	
Comparator supply voltage	V_{DD33}	-		2.97	3.3	3.63	V
Digital supple voltage	V_{DD09}	-		0.81	0.9	0.99	V
Temperature range	T_j	-		-40	+85	+150	°C
Input clock frequency	F_{CLK}	-		0.1	-	80	MHz
Operating clock frequency	F_{CLK_O}	-		0.1	2.5	10	MHz
Analog input voltage range	V_{IN}	-		0.06*V_{DDIO}	-	V_{DDIO}	V
Resolution threshold	N	-		-	8	-	bit
Programming threshold	V_{TH}	-		0	-	V_{DDIO}	V
Current consumption	I_{CC}	@VDDIO	Option 5V	-	0.28	0.30	mA
			Option 3.3V	-	0.26	0.30	
		@VDD33		-	0.05	0.05	
		@VDD09		-	3.16	24	uA
Standby current consumption	I_{STB}	@VDDIO	Option 5V	-	4.3	387	nA
			Option 3.3V	-	2.5	387	
		@VDD33		-	0.05	8	
		@VDD09		-	80	20920	
Conversion/Response rising time	T_R	@Vth = from 8 to 248		25.2	-	25.9	ns
Conversion/Response falling time	T_F	@Vth = from 8 to 248		25.2	-	25.8	ns
Delay between input clock and output rising time	PDr	@Vth = from 8 to 248		0.5	-	1.7	ns
Delay between input clock and output falling time	PDf	@Vth = from 8 to 248		0.5	-	1.4	ns