4-Channel GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS S/L1/L2/L3/L5 bands RF Front-End IC

1. OVERVIEW

NT1068 is 4-channel RF Front-End IC that covers all Global Navigation Satellite Systems (GPS, GLONASS, Galileo, BeiDou, NavIC, QZSS) as well as satellite-based augmentation systems like OmniSTAR at all frequency bands in various combinations: S, L1, L2, L3, L5, E1, E5a, E5b, E6, B1, B2, B3. NT1068 inherits all features of NT1065 including pin-to-pin compatibility. The key benefit of NT1068 over NT1065 is an ability to downconvert signals in S-band. There is a special configuration to acquire signals of S+L2 bands and L1+L3/L5 bands by single chip. It is also possible to obtain Galileo E5 band as well as BeiDou B1, B2, B3 (phase 3) band as entire signal with two channels fed by the same LO and then restore in digital domain to true complex data. As a benefit one can discover wide possibilities of improving the positioning accuracy down to centimeter range without taking RTK technique. NT1068 has the same channel structure as NT1065 with single conversion low-IF architecture. Each setting, including output signal frequency bandwidth, AGC options, mirror channel suppression option, etc., can be set for every channel individually. NT1068 does also integrate two fully independent frequency synthesizers that have the common reference (TCXO) input making LO signals coherent in terms of frequency. Channel#1 and channel#2 are supplied with common LO signal or two different LO signals generated in PLL “A” while PLL “B” is assigned for channels #3 and #4. For specific applications there is an option to feed all four channels with single LO source from PLL “A”.

2. FEATURES

- S, L1, L2, L3, L5 bands single conversion super heterodyne receiver with low-IF architecture
- Four independent configurable channels, each includes preamplifier, image rejection mixer, IF filter, IFA, 2-bit ADC
- Signal bandwidth up to 31MHz supports GNSS high precision codes such as P-code in GPS or wideband E5 Galileo
- Dual adoptable AGC system (RF + IF) or programmable gain
- High dynamic range with 1dB compression point more than –30dBm
- Analog differential output with two options of voltage swing 0.2/0.47Vp-p and 0.4/0.98Vp-p (sine wave/noise) or 2-bit ADC digital output data
- Two independent fully integrated synthesizers with flexible LO and CLK frequencies selection (“A” and “B”)
- Embedded temperature sensor
- SPI interface with easy-to-use register map
- Individual status indicators of main subsystems (available in SPI registers) and cumulative status indicator (AOK, available both as a separate pin and in SPI registers)
- Two form-factors: 6.0×6.5mm WLCSP and 10×10mm QFN88 package

3. APPLICATIONS

- GNSS based positioning systems
- GNSS based goniometric systems
- In-vehicle navigation systems
- GNSS based driverless car systems
- Professional drones

4. DESCRIPTION

4.1. BLOCK DIAGRAM

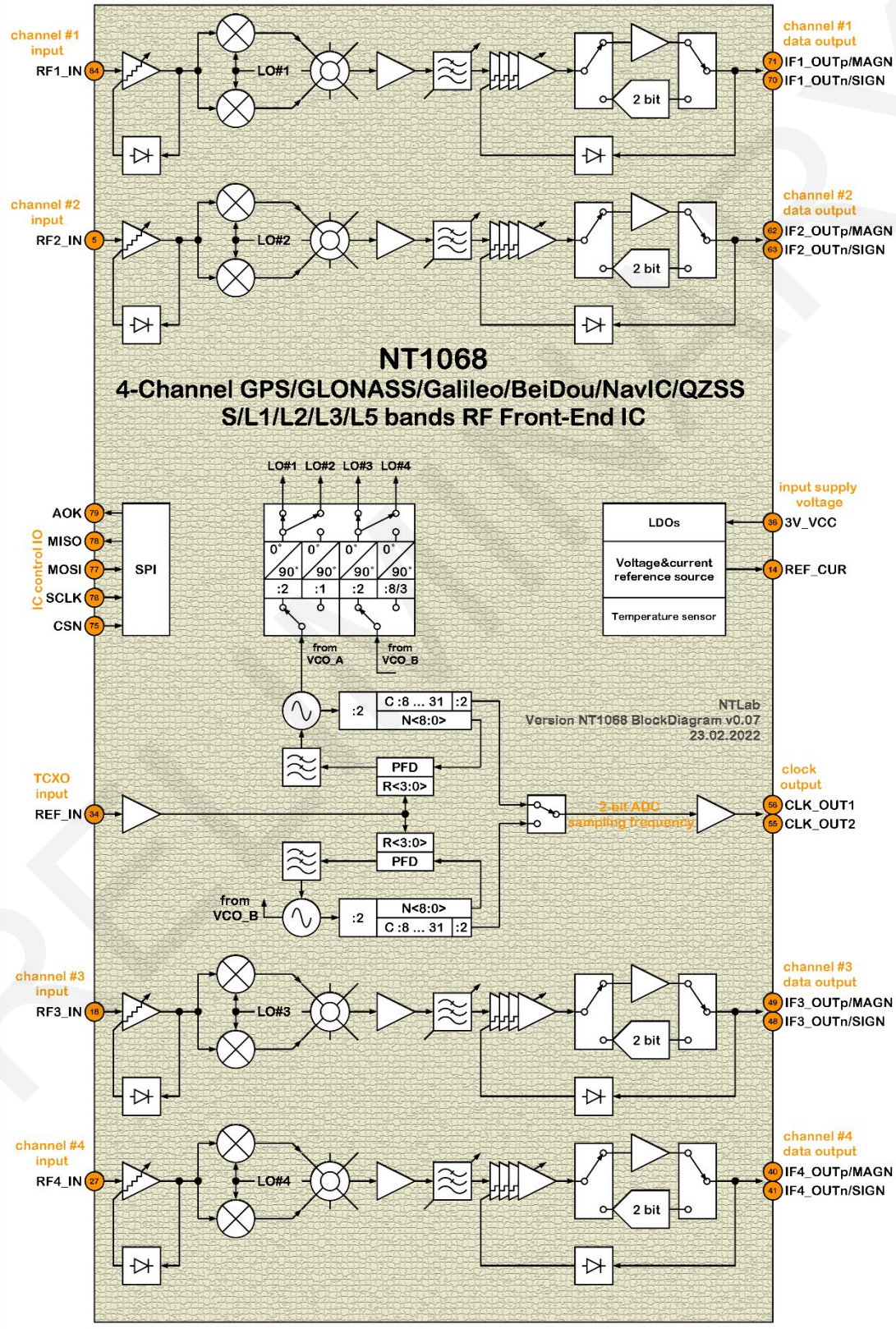


Figure 4.1: NT1068 Block diagram

4.2. APPLICATION SCHEMATIC

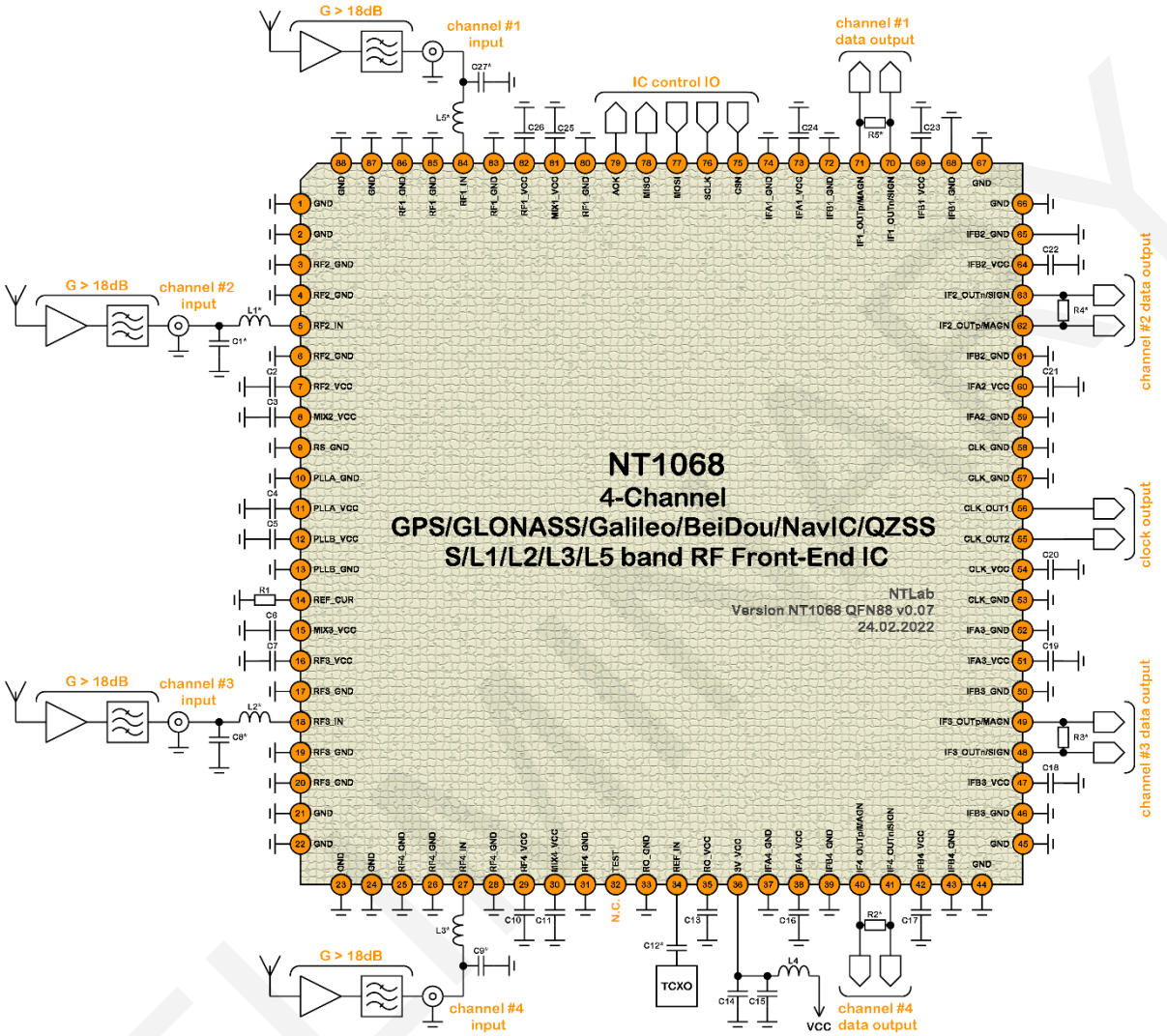


Figure 4.2: NT1068 QFN88 application schematic compatible to NT1065

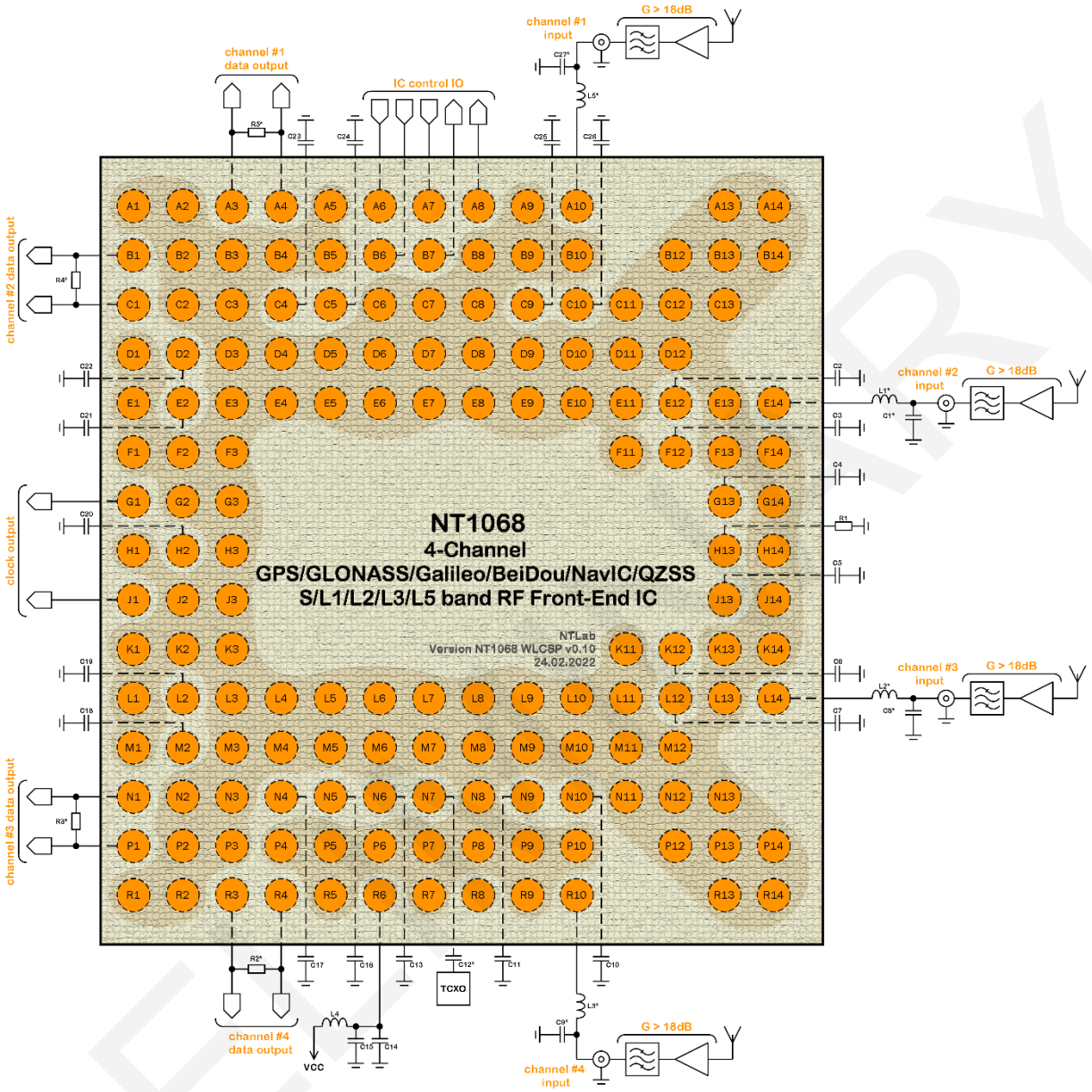


Figure 4.3: NT1068 WLCSP (top view) application schematic

Note: WLCSP balls that are not specified on Figure 4.3 (shaded area) except R8 must be connected to the ground.

Table 4.1: External components description

Component	Nominal value	Tolerance	Notes
C1[1]	2.2pF	±5%	Matching network capacitor for L1 band
	2.4pF	±5%	Matching network capacitor for L2/L3/L5 band
	1.5pF	±5%	Matching network capacitor for S band
C2	1µF	±20%	Supply voltage filter capacitor
C3	1µF	±20%	Supply voltage filter capacitor
C4	1µF	±20%	Supply voltage filter capacitor
C5	1µF	±20%	Supply voltage filter capacitor
C6	1µF	±20%	Supply voltage filter capacitor
C7	1µF	±20%	Supply voltage filter capacitor

Component	Nominal value	Tolerance	Notes
C8[1]	2.2pF	±5%	Matching network capacitor for L1 band
	2.4pF	±5%	Matching network capacitor for L2/L3/L5 band
	1.5pF	±5%	Matching network capacitor for S band
C9[1]	2.2pF	±5%	Matching network capacitor for L1 band
	2.4pF	±5%	Matching network capacitor for L2/L3/L5 band
	1.5pF	±5%	Matching network capacitor for S band
C10	1µF	±20%	Supply voltage filter capacitor
C11	1µF	±20%	Supply voltage filter capacitor
C12[1]	33pF	±20%	Blocking capacitor
C13	1µF	±20%	Supply voltage filter capacitor
C14	10nF	±20%	Supply voltage filter capacitor
C15	10µF	±20%	Supply voltage filter capacitor
C16	1µF	±20%	Supply voltage filter capacitor
C17	1µF	±20%	Supply voltage filter capacitor
C18	1µF	±20%	Supply voltage filter capacitor
C19	1µF	±20%	Supply voltage filter capacitor
C20	1µF	±20%	Supply voltage filter capacitor
C21	1µF	±20%	Supply voltage filter capacitor
C22	1µF	±20%	Supply voltage filter capacitor
C23	1µF	±20%	Supply voltage filter capacitor
C24	1µF	±20%	Supply voltage filter capacitor
C25	1µF	±20%	Supply voltage filter capacitor
C26	1µF	±20%	Supply voltage filter capacitor
C27[1]	2.2pF	±5%	Matching network capacitor for L1 band
	2.4pF	±5%	Matching network capacitor for L2/L3/L5 band
	1.5pF	±5%	Matching network capacitor for S band
L1[1]	6.8nH (Q≥40)	±2%	Matching network inductor for L1 band
	12nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	2.4nH (Q≥40)	±2%	Matching network inductor for S band
L2[1]	6.8nH (Q≥40)	±2%	Matching network inductor for L1 band
	12nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	2.4nH (Q≥40)	±2%	Matching network inductor for S band
L3[1]	6.8nH (Q≥40)	±2%	Matching network inductor for L1 band
	12nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	2.4nH (Q≥40)	±2%	Matching network inductor for S band
L4	120Ohm / 100MHz	±20%	Supply voltage filter inductor
L5[1]	6.8nH (Q≥40)	±2%	Matching network inductor for L1 band
	12nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	2.4nH (Q≥40)	±2%	Matching network inductor for S band
R1	61.9kOhm	±1%	High precision resistor
R2[1]	200Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R3[1]	200Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R4[1]	200Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output

Component	Nominal value	Tolerance	Notes
R5[1]	200Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output

Note 1: Defined depending on PCB construction and purpose

4.3. PINS DESCRIPTION

Note: WLCSP balls that are not listed in Table 4.2 must be connected to the ground.

Table 4.2: NT1068 pins description

Pin	Ball	Name	Description
1	A14	GND	Ground
2		GND	Ground
3	B14	RF2_GND	2nd channel RF ground
4		RF2_GND	2nd channel RF ground
5	E14	RF2_IN	2nd channel RF input (DC coupled)
6	C13	RF2_GND	2nd channel RF ground
7	E12	RF2_VCC	2nd channel “RF2” LDO output voltage 2.7V
8	F12	MIX2_VCC	2nd channel “MIX2” LDO output voltage 2.7V
9	F13	RS_GND	Voltage and current reference source ground
10	G14	PLLA_GND	PLL “A” ground
11	G13	PLLA_VCC	PLL “A” LDO output voltage 2.7V
12	J13	PLLB_VCC	PLL “B” LDO output voltage 2.7V
13	J14	PLLB_GND	PLL “B” ground
14	H13	REF_CUR	External high-precision resistor connection
15	K12	MIX3_VCC	3rd channel “MIX3” LDO output voltage 2.7V
16	L12	RF3_VCC	3rd channel “RF3” LDO output voltage 2.7V
17	N13	RF3_GND	3rd channel RF ground
18	L14	RF3_IN	3rd channel RF input (DC coupled)
19	P14	RF3_GND	3rd channel RF ground
20		RF3_GND	3rd channel RF ground
21	R14	GND	Ground
22		GND	Ground
23		GND	Ground
24		GND	Ground
25	R13	RF4_GND	4th channel RF ground
26		RF4_GND	4th channel RF ground
27	R10	RF4_IN	4th channel RF input (DC coupled)
28	P12	RF4_GND	4th channel RF ground
29	N10	RF4_VCC	4th channel “RF4” LDO output voltage 2.7V
30	N9	MIX4_VCC	4th channel “MIX4” LDO output voltage 2.7V
31	–	RF4_GND	4th channel RF ground
32	R8	TEST	Test output; should be opened
33	N8	RO_GND	Reference oscillator ground
34	N7	REF_IN	Reference frequency (TCXO) input
35	N6	RO_VCC	“RO” LDO output voltage 2.7V
36	R6	3V_VCC	Supply voltage 3V
37	P5	IFA4_GND	4th channel IFA ground
38	N5	IFA4_VCC	4th channel “IFA4” LDO output voltage 2.7V
39	R5	IFB4_GND	4th channel IF buffer & ADC ground
40	R4	IF4_OUTp/MAGN	4th channel analog output – true; 2-bit ADC digital output data – MAGN
41	R3	IF4_OUTn/SIGN	4th channel analog output – complement; 2-bit ADC digital output data – SIGN

Pin	Ball	Name	Description
42	N4	IFB4_VCC	4th channel "IFB4" LDO output supply 2.7V
43	R2	IFB4_GND	4th channel IF buffer & ADC ground
44	R1	GND	Ground
45		GND	Ground
46	N2	IFB3_GND	3rd channel IF buffer & ADC ground
47	M2	IFB3_VCC	3rd channel "IFB3" LDO output supply 2.7V
48	P1	IF3_OUTn/SIGN	3rd channel analog output – complement; 2-bit ADC digital output data – SIGN
49	N1	IF3_OUTp/MAGN	3rd channel analog output – true; 2-bit ADC digital output data – MAGN
50	M1	IFB3_GND	3rd channel IF buffer & ADC ground
51	L2	IFA3_VCC	3rd channel "IFA3" LDO output voltage 2.7V
52	L1	IFA3_GND	3rd channel IFA ground
53	K1	CLK_GND	CLK management unit ground
54	H2	CLK_VCC	"CLK" LDO output voltage 1.7V...VCC (Reg12<D4–D0> dependent)
55	J1	CLK_OUT2	Clock frequency analog output – complement
56	G1	CLK_OUT1	Clock frequency analog output – true; CMOS output
57	F1	CLK_GND	CLK management unit ground
58		CLK_GND	CLK management unit ground
59	E1	IFA2_GND	2nd channel IFA ground
60	E2	IFA2_VCC	2nd channel "IFA2" LDO output voltage 2.7V
61	D1	IFB2_GND	2nd channel IF buffer & ADC ground
62	C1	IF2_OUTp/MAGN	2nd channel analog output – true; 2-bit ADC digital output data – MAGN
63	B1	IF2_OUTn/SIGN	2nd channel analog output – complement; 2-bit ADC digital output data – SIGN
64	D2	IFB2_VCC	2nd channel "IFB2" LDO output voltage 2.7V
65	C2	IFB2_GND	2rd channel IF buffer & ADC ground
66	A1	GND	Ground
67		GND	Ground
68	A2	IFB1_GND	1st channel IF buffer & ADC ground
69	C4	IFB1_VCC	1st channel "IFB1" LDO output voltage 2.7V
70	A3	IF1_OUTn/SIGN	1st channel analog output – complement; 2-bit ADC digital output data – SIGN
71	A4	IF1_OUTp/MAGN	1st channel analog output – true; 2-bit ADC digital output data – MAGN
72	A5	IFB1_GND	1st channel IF buffer & ADC ground
73	C5	IFA1_VCC	1st channel "IFA1" LDO output voltage 2.7V
74	B5	IFA1_GND	1st channel IFA ground
75	A6	CSN	SPI chip select (active low)
76	B6	SCLK	SPI clock input
77	A7	MOSI	SPI data input
78	B7	MISO	SPI data output
79	A8	AOK	Cumulative status indicator: "1" valid "0" fail

Pin	Ball	Name	Description
80	–	RF1_GND	1st channel RF ground
81	C9	MIX1_VCC	1st channel "MIX1" LDO output voltage 2.7V
82	C10	RF1_VCC	1st channel "RF1" LDO output voltage 2.7V
83	B12	RF1_GND	1st channel RF ground
84	A10	RF1_IN	1st channel RF input (DC coupled)
85	A13	RF1_GND	1st channel RF ground
86		RF1_GND	1st channel RF ground
87	A14	GND	Ground
88		GND	Ground

Note: WLCSP balls that are not listed in Table 4.3 must be connected to the ground.

Table 4.3: NT1068 balls description

Ball	Pin	Name	Description
A3	70	IF1_OUTn/SIGN	1st channel analog output – complement; 2-bit ADC digital output data – SIGN
A4	71	IF1_OUTp/MAGN	1st channel analog output – true; 2-bit ADC digital output data – MAGN
A6	75	CSN	SPI chip select (active low)
A7	77	MOSI	SPI data input
A8	79	AOK	Cumulative status indicator: "1" valid "0" fail
A10	84	RF1_IN	1st channel RF input (DC coupled)
B1	63	IF2_OUTn/SIGN	2nd channel analog output – complement; 2-bit ADC digital output data – SIGN
B6	76	SCLK	SPI clock input
B7	78	MISO	SPI data output
C1	62	IF2_OUTp/MAGN	2nd channel analog output – true; 2-bit ADC digital output data – MAGN
C4	69	IFB1_VCC	1st channel "IFB1" LDO output voltage 2.7V
C5	73	IFA1_VCC	1st channel "IFA1" LDO output voltage 2.7V
C9	81	MIX1_VCC	1st channel "MIX1" LDO output voltage 2.7V
C10	82	RF1_VCC	1st channel "RF1" LDO output voltage 2.7V
D2	64	IFB2_VCC	2nd channel "IFB2" LDO output voltage 2.7V
E2	60	IFA2_VCC	2nd channel "IFA2" LDO output voltage 2.7V
E12	7	RF2_VCC	2nd channel "RF2" LDO output voltage 2.7V
E14	5	RF2_IN	2nd channel RF input (DC coupled)
F12	8	MIX2_VCC	2nd channel "MIX2" LDO output voltage 2.7V
G1	56	CLK_OUT1	Clock frequency analog output – true; CMOS output
G13	11	PLLA_VCC	PLL "A" LDO output voltage 2.7V
H2	54	CLK_VCC	"CLK" LDO output voltage 1.7V...VCC (Reg12<D4–D0> dependent)
H13	14	REF_CUR	External high-precision resistor connection
J1	55	CLK_OUT2	Clock frequency analog output – complement
J13	12	PLLB_VCC	PLL "B" LDO output voltage 2.7V
K12	15	MIX3_VCC	3rd channel "MIX3" LDO output voltage 2.7V

Ball	Pin	Name	Description
L2	51	IFA3_VCC	3rd channel “IFA3” LDO output voltage 2.7V
L12	16	RF3_VCC	3rd channel “RF3” LDO output voltage 2.7V
L14	18	RF3_IN	3rd channel RF input (DC coupled)
M2	47	IFB3_VCC	3rd channel “IFB3” LDO output supply 2.7V
N1	49	IF3_OUTp/MAGN	3rd channel analog output – true; 2-bit ADC digital output data – MAGN
N4	42	IFB4_VCC	4th channel “IFB4” LDO output supply 2.7V
N5	38	IFA4_VCC	4th channel “IFA4” LDO output voltage 2.7V
N6	35	RO_VCC	“RO” LDO output voltage 2.7V
N7	34	REF_IN	Reference frequency (TCXO) input
N9	30	MIX4_VCC	4th channel “MIX4” LDO output voltage 2.7V
N10	29	RF4_VCC	4th channel “RF4” LDO output voltage 2.7V
P1	48	IF3_OUTn/SIGN	3rd channel analog output – complement; 2-bit ADC digital output data – SIGN
R3	41	IF4_OUTn/SIGN	4th channel analog output – complement; 2-bit ADC digital output data – SIGN
R4	40	IF4_OUTp/MAGN	4th channel analog output – true; 2-bit ADC digital output data – MAGN
R6	36	3V_VCC	Supply voltage 3V
R8	32	TEST	Test output; should be opened
R10	27	RF4_IN	4th channel RF input (DC coupled)

4.4. SERIAL INTERFACE DESCRIPTION

4.4.1. PROTOCOL DESCRIPTION

NT1068 can be configured with standard 4-wire SPI. In addition special pin "AOK" (cumulative status indicator) for unexpected system failure tracking is available.
User register map is split up into five parts according to functionality:

- System Info
- General settings and status
- CLK settings
- Channel settings and status (separate for each channel)
- PLL settings and status (separate for each PLL)

Available settings and statuses are listed in subsection 4.4.2.

4.4.1.1. GENERAL DESCRIPTION

Serial interface is used to read and change NT1068 data register information. It is intended for status monitoring, mode configuration and parameter adjustment.
Serial interface uses 4 pin for communication:

- CSN – serial interface enable chip select signal (low active)
- MISO – serial interface output data
- MOSI – serial interface input data
- SCLK – serial interface clock (low when idle)

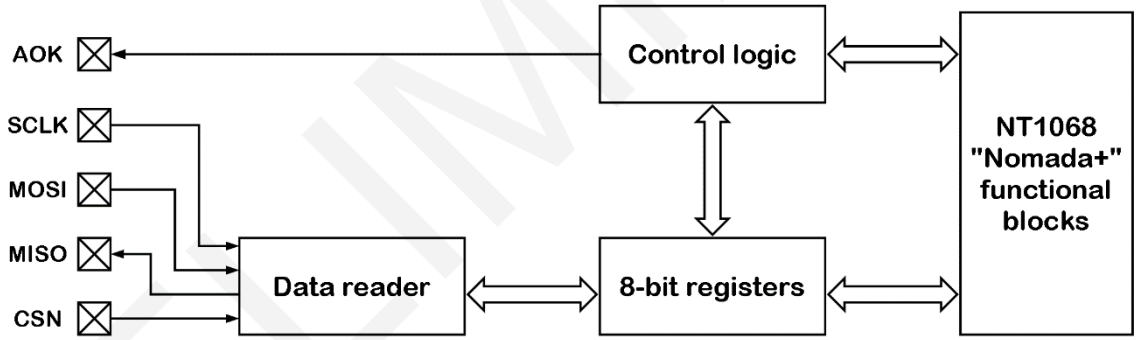


Figure 4.4: Serial interface structure

Standard information packet (command) consists of two bytes. The first byte is command/address, second – data byte. Data format is always a bit sequence from first MSB to last LSB. All data transfers are framed by CSN signal, which must be low for any data transfer. In "idle" state, when CSN is high, SCLK, MOSI and MISO pins are blocked and don't respond to external signals. At the beginning of any data transfer (falling CSN edge) SCLK must be low.

4.4.1.2. WRITING TO REGISTER

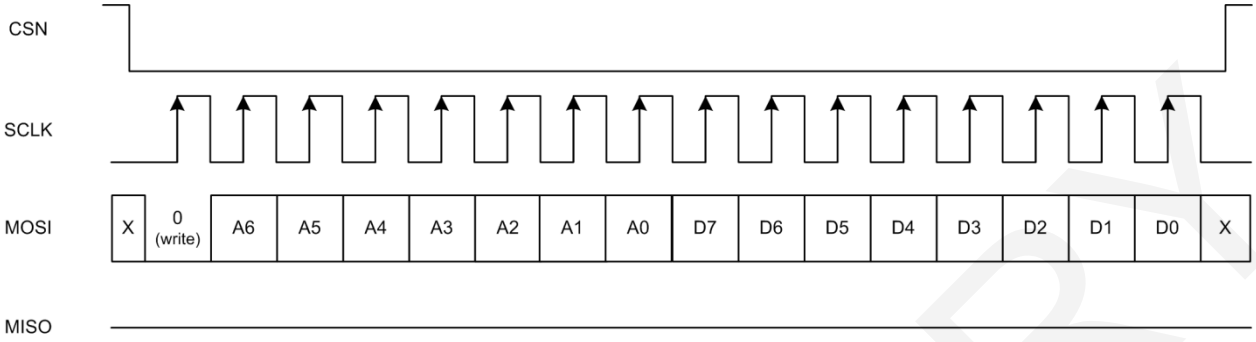


Figure 4.5: Individual register writing

Single write reading is shown on Figure 4.5. Communication is initialized by setting Chip Select (CSN) pin low. Bytes are transmitted MSB first. Data are clocked into the NT1068, through the MOSI pin, on the rising edges of SCLK. The first bit of a command/address byte is a read/write attribute: read operation is defined by logic "1" and write operation is defined by logic "0". Bits A6…A0 represent the address of the register to be read or written. Second byte (D7…D0 bits) is data written to the given address register. After the 16th rising SCLK edge and turn-off CSN hold time CSN goes high, disabling the interface.

4.4.1.3. READING FROM REGISTER

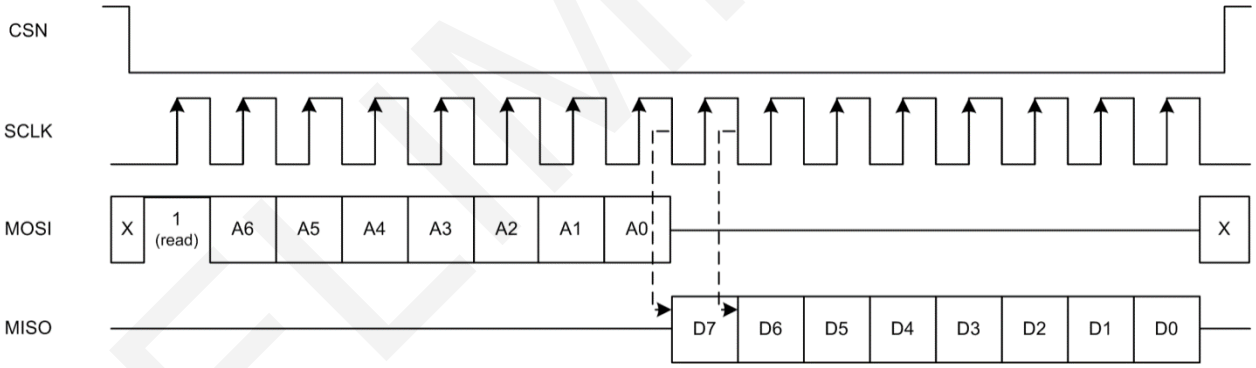


Figure 4.6: Single register reading

Single register reading is similar to writing. First byte is command byte. Read attribute is logic "1" and A6…A0 bits specify address of register to be read. Data are clocked out the NT1068, through the MISO pin, on the falling edges of SCLK. Output data should be clocked on rising SCLK edges of external SPI master. Bytes are transmitted MSB first. After sending data byte CSN goes high, disabling the interface.

4.4.1.4. BURST DATA TRANSFER

The NT1068 has a SPI burst-mode data transfer. Unlike single data transfer CSN is continue to be “low” after LSB of data byte. Next bit after LSB is a write/read attribute. CSN goes high to stop burst data transfer. Direction of data transfer can be changed an infinite number of times during burst data transfer. See examples below, please.

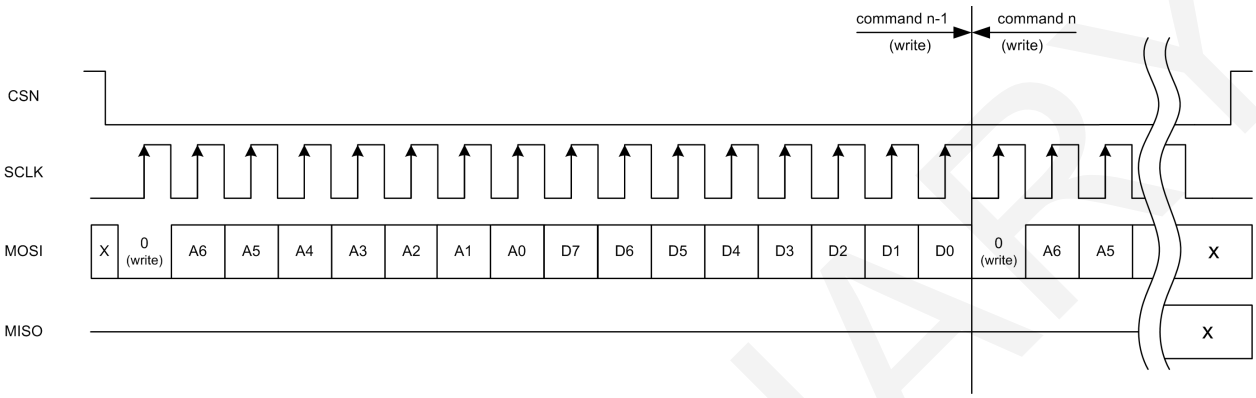


Figure 4.7: Burst data writing

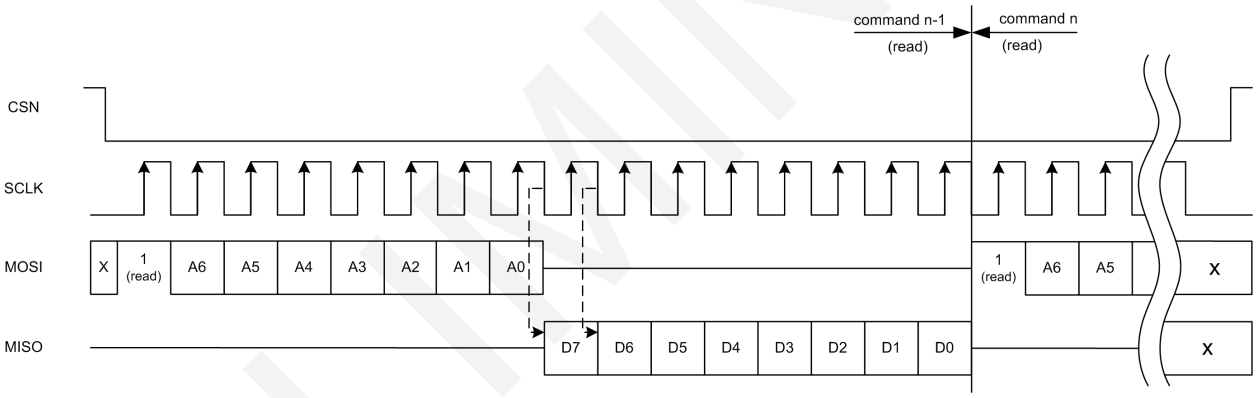


Figure 4.8: Burst data reading

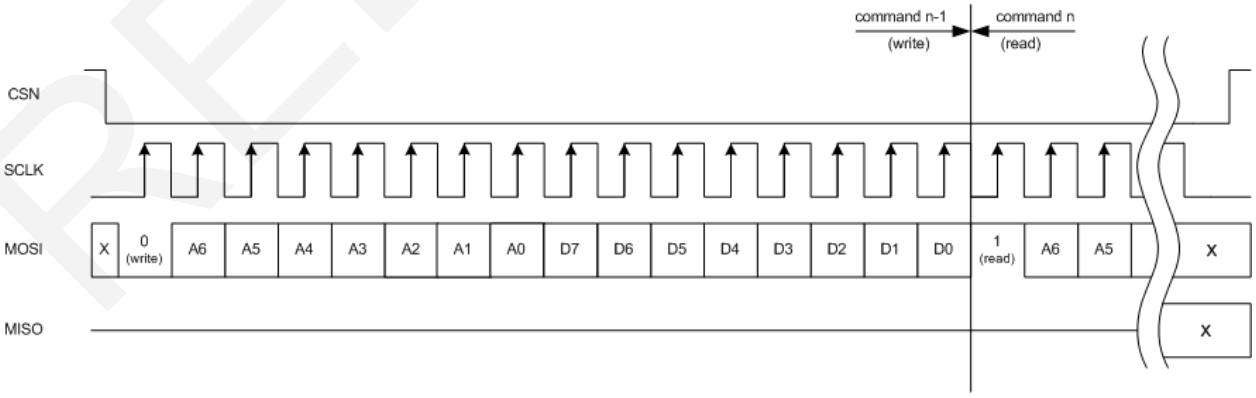


Figure 4.9: Burst data writing and reading

4.4.1.5. TIMING DIAGRAM

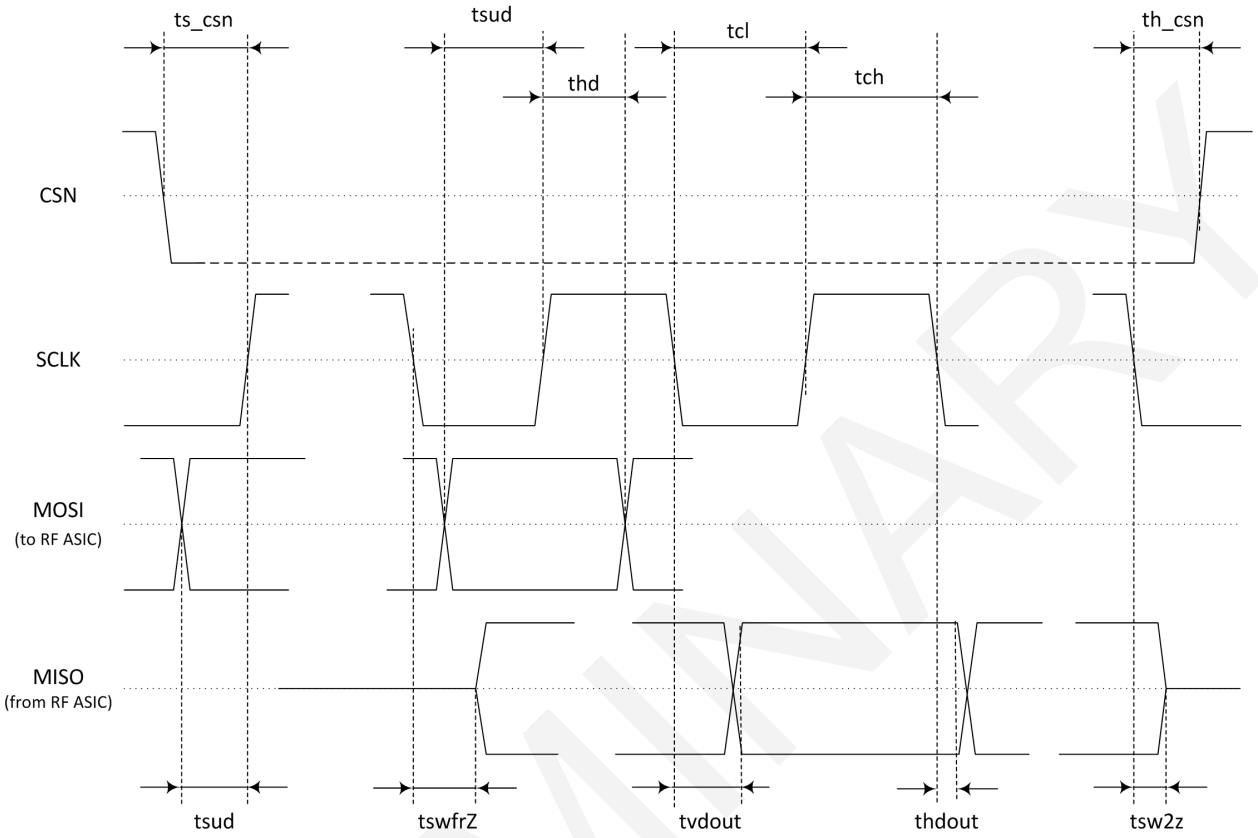


Figure 4.10: SPI timing diagram

Table 4.4: SPI timing

Parameter description	Symbol	Condition	Value			Unit
			min	typ.	max	
SCLK frequency	fclk	–	–	–	40	MHz
SCLK high and low time	tch tcl	1/fclk = (tch+tcl)	8	–	12	ns
Duty cycle	D	–	40	–	60	%
CSN setup time before SCLK	ts_csn	–	8	–	–	ns
CSN hold time	th_csn	–	4	–	–	ns
Data set up time	tsud	–	10	–	–	ns
Data hold time	thd	–	3	–	–	ns
Switch from Z-state time	tswfrZ	Load 20 pF	–	–	10	ns
Output data hold time	thdout	Load 20 pF	2.8	–	–	ns
Output data valid time	tvdout	Load 20 pF	–	–	10	ns
Switch to Z-state time	tsw2z	Load 20 pF	3	–	8	ns

4.4.2. PROGRAMMABLE REGISTERS

4.4.2.1. SYSTEM INFO

– ID number, release

Bit number	Name	Description	Default
Reg0, 0x00			
D7–D0	ID<12:5>	Technical information. Chip number. $(0010000101100)_{dec}$ = 1068	"00100001"
Reg1, 0x01			
D7–D3	ID<4:0>	Continue. Refer to Reg0<D7–D0>	"01100"
D2–D0	Release<2:0>	Technical information. Chip version. $(001)_{dec}$ =1	"001"

4.4.2.2. GENERAL SETTINGS AND STATUS

– Mode (standby, synthesizer only, active)
– TCXO frequency setting
– LO source (PLL "A" for all channels; PLL "A" for channels#1&2 + PLL "B" for channels#3&4)
– LPF autocalibration system execute and status
– Channel# to be monitored for status (ch#1, ch#2, ch#3, ch#4)
– Temperature measurement mode (single, continuous)
– Temperature measurement system execute
– AOK indicator configuration
– General status (AOK, temperature)
– Selected channel status (RF AGC indicator, RF gain, IG gain)

Bit number	Name	Description	Default
Reg2, 0x02			
D7–D2	Unused	Unused	"000000"
D1–D0	Mode<1:0>	IC mode: "00" standby "01" PLL "A" only "10" PLL "A" only "11" active **Note:** As register bits are writable in any mode, exclude any configuration change in "standby" mode to return in last configured "active" mode.	"11"
Reg3, 0x03			
D7	Unused	Unused	"0"
D6–D1	TCXO_sel<5:0>	TCXO frequency setting: "000000" 10 MHz "000001" 24.84 MHz "000010" 4.688 … 5.312 MHz … … "001000" 4.688 … 5.312 MHz … with step of 0.625MHz "110000" 29.688 … 30.312 MHz "110001" 30.313 … 30.937 MHz not guaranteed … with step of 0.625MHz "111111" 39.063 … 39.687 MHz not guaranteed	"000000"
D0	LO_Source	LO source: "0" PLL "A" for all channels "1" PLL "A" for channels#1&2, PLL "B" for channels#3&4	"1"

Bit number	Name	Description	Default
Reg4, 0x04			
D7–D2	Unused	Unused	"000000"
D1	LPF_ACS_S	LPF autocalibration system status: "0" error "1" completed successfully	–
D0	LPF_EXE	LPF auto-calibration system execute (duration is about 15 ms and it automatically resets to "0" when finished): "0" finished "1" start	"1"
Reg5, 0x05			
D7–D6	Unused	Unused	"00"
D5–D4	Ch_StNumSel<1:0>	Channel to be monitored for status: "00" channel#1 "01" channel#2 "10" channel#3 "11" channel#4	"00"
D3–D2	Unused	Unused	"00"
D1	TS_MD	Temperature measurement mode: "0" single "1" continuous	"0"
D0	TS_EXE	Temperature measurement system execute (duration is up to 17 ms and it automatically resets to "0" when finished): "0" finished "1" start	"0"
Reg6, 0x06			
D7–D5	Unused	Unused	"000"
D4	LPF_ACS_AOK	LPF autocalibration system status as AOK's component: "0" forbidden "1" permitted	"1"
D3	PLL_LI_AOK	PLL "A" & "B" (if enabled) lock indicator as AOK's components: "0" forbidden "1" permitted	"1"
D2	PLL_VCO_AOK	PLL "A" & "B" (if enabled) VCO input voltage comparator status as AOK's component: "0" forbidden "1" permitted	"1"
D1	RF_AGC_AOK	RF AGC indicators (all enabled channels) as AOK's components: "0" forbidden "1" permitted	"0"
D0	StdBy_AOK	IC standby mode as AOK's component (forces AOK to "0" in standby mode): "0" forbidden "1" permitted	"1"
Reg7, 0x07			
D7–D5	Unused	Unused	"000"
D4	AOK	Cumulative status indicator: "0" fail "1" valid	–

Bit number	Name	Description	Default
D3–D2	Unused	Unused	"00"
D1–D0	TS_code<9:8>	Temperature sensor indicator: "0000000000" not valid range … "0110010100" not valid range "0110010101" +125 °C $Temp = 417.2 - 0.722 * (TS\_code < 9:0 >)_{dec}$ … "1001111001" –40 °C "1001111010" not valid range … "1111111111" not valid range	–
Reg8, 0x08			
D7–D0	TS_code<7:0>	Continue. Refer to Reg7<D1–D0>	–
Reg9, 0x09			
D7–D6	Unused	Unused	"00"
D5–D4	RF_AGC_Down RF_AGC_Up	RF AGC indicator (refer to Reg5<D5–D4> for channel selection): "00" input signal power is within regulating range "01" input signal power is lower than threshold "10" input signal power is higher than regulating range "11" impossible state or RF AGC system is damaged	–
D3–D0	RF_GainSt<3:0>	RF gain value (refer to Reg5<D5–D4> for channel selection) "0000" 5 dB … with step of 0.95 dB "1111" 19.5 dB	–
Reg10, 0x0A			
D7–D5	Unused	Unused	"000"
D4–D0	IFA_GainSt<4:0>	IFA gain value at T = +25 °C (refer to Reg5<D5–D4> for channel selection): "00000" –0.5 dB … … "00011" 10.5 dB … … "00111" 22.7 dB … … "01010" 31.5 dB … … "01110" 41.0 dB … … "10001" 50.7 dB … … "10101" 61.0 dB … … "10111" 63.0 dB "11000" not valid range … not valid range "11111" not valid range	–

4.4.2.3. CLK SETTINGS

- CLK C-divider ratio (:8, :9 … :31)
- CLK output disable
- CLK frequency source (PLL "A", PLL "B")
- CLK type (differential LVDS-like, CMOS)

- CLK amplitude (230mV, 340mV, 450mV, 560mV if differential LVDS-like type; 1.8V, 2.4V, 2.7V, VCC if CMOS type)
- CLK output DC level (1.5V, 2.1V, 2.4V, 2.7V) //if differential LVDS-like type

Bit number	Name	Description	Default
Reg11, 0x0B			
D7–D5	Unused	Unused	"000"
D4–D0	CDIV_R<4:0>	CLK C-divider ratio (refer to formula in section 7.8 for F_{CLK} calculation): "01000" 8 … with step of 1 "11111" 31	"01111"
Reg12, 0x0C			
D7	Unused	Unused	"00"
D6	CLK_OFF	CLK output: "0" enabled "1" disabled	"0"
D5	CLK_Source	CLK frequency source: "0" from PLL "A" "1" from PLL "B"	"0"
D4	CLK_TP	CLK type: "0" CMOS "1" differential LVDS-like	"1"
D3–D2	CLK_CC<1:0>	CLK amplitude with R_{load} / without R_{load} if differential LVDS-like type (V_{pp}) : "00" 0.23 / 0.46V "01" 0.34 / 0.69 V "10" 0.45 / 0.92 V "11" 0.56 / 1.13 V	"10"
D1–D0	CLK_OL<1:0>	CLK output logic-level high if CMOS type (refer to Reg12<D4>): "00" 1.8 V "01" 2.4 V "10" 2.7 V "11" external (VCC) CLK output DC level if differential LVDS-like type (refer to Reg12<D4>): "00" (1.8 – 0.55×V_{pp}) V "01" (2.4 – 0.55×V_{pp}) V "10" (2.7 – 0.55×V_{pp}) V "11" (VCC – 0.55×V_{pp}) V	"00"

4.4.2.4. CHANNEL SETTINGS

- Channel enable
- Channel mode (lower sideband, upper sideband)
- IF passband (7 bits, 15 – 31MHz)
- Output data interface (analog differential output, 2-bit ADC output)
- IFA output DC level (1.55V, 1.75V, 1.90V, 2.0V)
- RF GC mode (manual, auto)
- IFA GC mode (manual, auto)
- RF AGC thresholds (3 bits for upper threshold, 3 bits for lower threshold)
- IF AGC threshold (200mV, 400mV)
- RF gain in manual mode (4 bits)
- IFA gain in manual mode (10 bits)
- IF AGC digital detector threshold
- Channel output load 200Ohm external resistor (yes, no)
- ADC output logic-level high (1.8V, 2.4V, 2.7V, VCC)
- ADC type (asynchronous, clocked by rising edge, clocked by falling edge)

Bit number	Name	Description	Default
Reg13, 0x0D for Channel#1 / Reg20, 0x14 for Channel#2 / Reg27, 0x1B for Channel#3 / Reg34, 0x22 for Channel#4			
D7–D2	Unused	Unused	“000000”
D1	Ch#_LSB	Channel# GNSS: “0” upper sideband “1” lower sideband	Ch#1&4 “1” Ch#2&3 “0”
D0	Ch#_EN	Channel# enable: “0” disabled “1” enabled	“1”
Reg14, 0x0E for Channel#1 / Reg21, 0x15 for Channel#2 / Reg28, 0x1C for Channel#3 / Reg35, 0x23 for Channel#4			
D7	Unused	Unused	“0”
D6–D0	LPF_code#<6:0>	IF passband: “0000000” 11.22 MHz not guaranteed range … … “0010101” 14.83 MHz not guaranteed range “0010110” 15.12 MHz … … “0011011” 16.59 MHz … … “0011110” 17.60 MHz … … “0100001” 18.33 MHz … … “0100100” 19.36 MHz … … “0100111” 20.31 MHz … … “0101010” 21.13 MHz … … “0101101” 21.92 MHz … … “0110000” 22.89 MHz … … “0110011” 23.82 MHz … … “0110110” 24.94 MHz … … “0111001” 25.45 MHz … … “0111100” 26.50 MHz … … “0111111” 27.38 MHz … … “1000010” 28.31 MHz … … “1000101” 29.02 MHz … … “1001000” 29.64 MHz … … “1001011” 30.47 MHz … … “1001101” 31.19 MHz “1001110” 31.55 MHz not guaranteed range … … “1111111” 43.41 MHz not guaranteed range	Ch#1 “1010010” Ch#2 “1001000’ Ch#3 “0111110” Ch#4 “0100000”

Bit number	Name	Description	Default
Reg15, 0x0F for Channel#1 / Reg22, 0x16 for Channel#2 / Reg29, 0x1D for Channel#3 / Reg36, 0x24 for Channel#4			
D7	Unused	Unused	"0"
D6	IFA#_AmpLvl	IF AGC threshold (w.r.t. sinewave signal): "0" 200 mV "1" 400 mV	"0"
D5	IFA#_ResLoad	Channel output load 200 Ohm external resistor: "0" not mounted "1" mounted	"1"
D4	RF#_AGC_MD	RF GC mode: "0" manual gain control (refer to RF#_Gain<3:0> to set gain) "1" automatic gain control (refer to RF#_AGC_UB<2:0> and RF#_AGC_LB<2:0> to set thresholds)	"0"
D3	IFA#_AGC_MD	IFA GC mode: "0" manual gain adjustment (refer to IFA#_ManGC<4:0> and IFA#_Gain<4:0> to set gain) "1" automatic gain control	"1"
D2–D1	IFA#_OP<1:0>	IFA output DC level (if IFA#_OT = "0"): "00" 1.55 V "01" 1.75 V "10" 1.90 V "11" 2.00 V	"01"
D0	IFA#_OT	Output data interface: "0" analog differential output "1" 2-bit ADC output (CMOS)	"0"
Reg16, 0x10 for Channel#1 / Reg23, 0x17 for Channel#2 / Reg30, 0x1E for Channel#3 / Reg37, 0x25 for Channel#4			
D7	Unused	Unused	"0"
D6–D4	RF#_AGC_UB<2:0>	RF AGC upper threshold (w.r.t. sinewave signal input power): "000" –42 dBm "001" –40 dBm "010" –38 dBm "011" –37 dBm "100" –36 dBm "101" –35 dBm "110" not valid range "111" not valid range	"011"
D3	Unused	Unused	"0"
D2–D0	RF#_AGC_LB<2:0>	RF AGC lower threshold (w.r.t. sinewave signal input power): "000" not valid range "001" not valid range "010" not valid range "011" –44 dBm "100" –41 dBm "101" –40 dBm "110" –38 dBm "111" –37 dBm	"100"
Reg17, 0x11 for Channel#1/ Reg24, 0x18 for Channel#2/ Reg31, 0x1F for Channel#3/ Reg38, 0x26 for Channel#4			
D7–D4	RF#_Gain<3:0>	RF gain in manual mode (if RF#_AGC_MD = "0"): "0000" 5 dB … with step of 0.95 dB "1111" 19.5 dB	"1111"

Bit number	Name	Description	Default
D3–D2	Unused	Unused	"00"
D1–D0	IFA#_ManGC<4:3>	IFA coarse gain value in manual mode (IFA#_AGC_MD = "0"): "00000" –0.5 dB "00011" 10.5 dB "00111" 22.7 dB "01010" 31.5 dB "01110" 41.0 dB "10001" 50.7 dB "10101" 61.0 dB "10111" 63.0 dB "11000" not valid range … not valid range "11111" not valid range	"01"
Reg18, 0x12 for Channel#1 / Reg25, 0x19 for Channel#2 / Reg32, 0x20 Channel#3 / Reg39, 0x27 for Channel#4			
D7–D5	IFA#_ManGC<2:0>	Continue. Refer to Reg17<D1–D0>	"111"
D4–D0	IFA#_Gain<4:0>	IFA fine gain value in manual mode (if IFA#_AGC_MD = "0"): "00000" –0.35 dB … … "00111" –0.35 dB "01000" –0.30 dB "01001" –0.10 dB "01010" 0.30 dB "01011" 0.90 dB "01100" 1.70 dB "01101" 2.40 dB "01110" 3.00 dB "01111" 3.40 dB "10000" 3.80 dB "10001" 4.10 dB "10010' 4.40 dB "10011" 4.55 dB "10100" 4.70 dB "10101" 4.80 dB "10110" 4.90 dB "10111" 5.00 dB "11000" 5.05 dB "11001" 5.10 dB … … "11111" 5.10 dB	IF AGC digital detector threshold w.r.t. sinewave signal (if IFA#_AGC_MD = "1") & (IFA#_OT = "1"): "00000" 0.2% … … "00100" 15.1% … … "01001" 27.8% "01010" 30.3% "01011" 32.4% "01100" 34.5% "01111" 41.0% "10000" 43.2% … … "10011" 49.8% … … "11000" 60.8% "11001" not valid range … not valid range "11111" not valid range	"01010"
Reg19, 0x13 for Channel#1 / Reg26, 0x1A for Channel#2 / Reg33, 0x21 for Channel#3 / Reg40, 0x28 for Channel#4			
D7–D4	Unused	Unused	"0000"
D3–D2	IFA#_ADC_Clk<1:0>	ADC type: "00" asynchronous "01" asynchronous "10" clocked by rising edge "11" clocked by falling edge	"10"
D1–D0	IFA#_ADC_OL<1:0>	ADC output logic-level high (if IFA#_OT<D0> = "1"): "00" 1.8 V "01" 2.4 V "10" 2.7 V "11" external (VCC)	"10"

4.4.2.5. PLL SETTINGS AND STATUS

- PLL enable
- Frequency band
- N-divider ratio (N<8:0>)
- R-divider ratio (R<3:0>)
- PLL tuning system execute
- Status (VCO input voltage comparator, lock indicator)

Bit number	Name	Description	Default
Reg41, 0x29 for PLL "A" / Reg45, 0x2D for PLL "B"			
D7–D3	Unused	Unused	"00000"
D2–D1	PLL_#_Band<1:0>	PLL# frequency band: PLL "A" / PLL "B" LO_source="0" / LO_source="1" "00" L2/L3/L5 / L2/L3/L5 — "00" L2/L3/L5 / LO_source="1" "01" L1 / L1 — "01" L1 / LO_source="1" "10" S / unused — "10" unused / LO_source="1" "11" unused / S for ch#1 + L2 for ch#2 — "11" L1 for ch#3 + L3/L5 for ch#4	PLL "A" "01" PLL "B" "00"
D0	PLL_#_EN	PLL# enable: "0" disabled "1" enabled	"1"
Reg42, 0x2A for PLL "A" / Reg46, 0x2E for PLL "B"			
D7–D0	NDiv_R_#<8:1>	PLL# N-divider ratio (refer to formula in section 7.2 for F_{LO} calculation): "000110000" 48 … with step of 1 "111111111" 511	PLL "A" "01001111" PLL "B" "01111011"
Reg43, 0x2B for PLL "A" / Reg47, 0x2F for PLL "B"			
D7	NDiv_R_#<0>	Continue. Refer to Reg42<D7–D0> / Reg46<D7–D0>	"1"
D6–D3	RDiv_R_#<3:0>	PLL# R-divider ratio (refer to formula in section 7.2 for F_{LO} calculation): "0001" 1 … with step of 1 "1111" 15	PLL "A" "0001" PLL "B" "0010"
D2–D1	Unused	Unused	"00"
D0	PLL_EXE_#	PLL# tuning system execute: "0" finished "1" start (reset to "0" automatically when finished)	"0"
Reg44, 0x2C for PLL "A" / Reg48, 0x30 for PLL "B"			
D7–D3	Unused	Unused	"00000"
D2–D1	Vco#_CVL Vco#_CVH	VCO input voltage indication: "00" valid "01" upper threshold exceeded (oscillation frequency is too low) "10" lower threshold exceeded (oscillation frequency is too high) "11" unused	–
D0	PLL_LI_#	PLL# lock indicator: "0" not locked "1" locked	–

5. OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage _____ –0.3…+ 3.6 V
Maximum input signal level _____ +10 dBm
Input pin voltage _____ –0.3… +3.6V
Storage temperature _____ –55…+125 °C
Soldering temperature _____ +260 °C
Electrostatic discharge rating (JESD78D Class II, Level A):

- HBM (pins 5, 18, 27, 84) _____ 0.5 kV
- HBM (pins 14, 34, 40, 41, 48, 49, 55, 56, 62, 63, 70, 71, 75–79) _____ 1 kV
- HBM (except pins 5, 14, 18, 27, 34, 40, 41, 48, 49, 55, 56, 62, 63, 70, 71, 75–79, 84) _____ 2 kV

5.1. DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.85V to 3.3V, T_A=–40…+85°C. Typical values are at V_{cc} = 3.0V, T_A=+25°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Supply voltage	V_{cc}	–		2.85	3.0	3.3	V
Current consumption	I_{cc}	Mode 1.1/Mode 1.2		–	37.3/33.6	–	mA
		Mode 2.1/Mode 2.2		–	57.5/50.2	–	
		Mode 3.1/Mode 3.2		–	64.9/57.6	–	
		Mode 4.1/Mode 4.2		–	99.1/84.3	–	
		Mode 5.1/Mode 5.2		–	105.4/90.7	–	
		Mode 6.1/Mode 6.2		–	89.8/78.5	–	
		Mode 7.1/Mode 7.2		–	110.8/95.8	–	
		Mode 8.1/Mode 8.2		–	100.9/85.9	–	
		Shutdown mode		–	0.8	3.5	uA
Input logic-level low	V_{IL}	–		0	–	0.3	V
Input logic-level high	V_{IH}	–		V_{cc} – 0.3	–	V_{cc}	V
Output logic-level low	V_{OL}	I_{LOAD} = 100uA		0	–	0.3	V
Output logic-level high	V_{OH}	I_{LOAD} = 100uA		V_{cc} – 0.3	–	V_{cc}	V
Output logic-level high (ADC output)	V_{OH_ADC}	I_{LOAD} = 0mA/2mA	Preset 1	–	1.8/1.7	–	V
			Preset 2	–	2.4/2.3	–	
			Preset 3	–	2.7/2.6	–	
			Preset 4	–	V_{cc} /V_{cc} – 0.2	–	
Output logic-level low (ADC output)	V_{OL_ADC}	I_{LOAD} =2mA		0	–	0.4	V
IFA output DC level	V_{DC_IFA}	Preset 1		–	1.56	–	V
		Preset 2		–	1.75	–	
		Preset 3		–	1.86	–	
		Preset 4		–	2.04	–	
Differential clock output DC level	V_{DC_CLK}	Preset 1		–	1.57	–	V
		Preset 2		–	2.17	–	
		Preset 3		–	2.45	–	
		Preset 4		–	2.63	–	
Die temperature measurement range	T_j	–		–40	25	+125	°C
Die temperature measurement accuracy	ΔT_j	–		–	±5	–	°C

Modes:
1. 1 channel (L1 or L2/L3/L5 band @ PLL “A”)
2. 2 channels (2 L1 or 2 L2/L3/L5 band @ PLL “A”)
3. 2 channels (L1 band @ PLL “A” + L2/L3/L5 band @ PLL “B”)
4. 4 channels (4 L1 or 4 L2/L3/L5 band @ PLL “A”)
5. 4 channels (2 L1 band @ PLL “A” + 2 L2/L3/L5 band @ PLL “B”)
6. 3 channels (S band @ PLL “A” + L1 band @ PLL “B” + L5 band @ PLL “B”)
7. 4 channels (S band @ PLL “A” + L2 band @ PLL “A” + L1 band @ PLL “B” + L5 band @ PLL “B”)
8. 4 channels (4 S band @ PLL “A”)

*.1. analog differential output, IF AGC threshold = 200mV
*.2. 2-bit ADC output, V_{OH_ADC} = 2.7V, C_{LOAD} = 5pF

5.2. AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.85V to 3.3V, T_A=–40…+85°C. Typical values are at V_{cc} = 3.0V, T_A =+25°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Overall							
Input frequency range	F_{IN}	L1 band		1530	–	1620	MHz
		L2/L3/L5 band		1150	–	1300	
		S band		2460	–	2530	
Reference frequency (TCXO) range	F_{REF}	–		5	10/24.84	30	MHz
Noise figure	NF_{RF_IN}	Note 1	L1 band	–	6.2	–	dB
			L2/L3/L5 band	–	6.8	–	
			S band	–	6.0	–	
1 dB compression point	$P_{1dB\_RF\_IN}$	Note 2		–	–23	–	dBm
		Note 3		–	–38	–	
Total gain	G_{MAX}	–		–	83	–	dB
Channel isolation	Ch_{ISO}	–		–	40	–	dB
Input VSWR	$VSWR_{RF\_IN}$	With matching circuit. @50Ohm	L1 band	–	1.5	2	–
			L2/L3/L5 band	–	1.8	2	
			S band	–	1.5	2	
RF AGC range	ΔG_{RF}	–		–	14.5	–	dB
IF AGC range	ΔG_{IF}	–		–	64	–	dB
Preamp&MIX							
Image rejection	IR	–		–	30	–	dB
RF (Preamp&Mixer) max gain	G_{MAX_RF}	–		–	19.5	–	dB
RF (Preamp&Mixer) min gain	G_{MIN_RF}	–		–	5	–	dB
Preamp gain step	G_{STEP_MIX}	–		–	0.95	–	dB
LPF&IFA							
Output frequency range	F_{IF}	Tunable, assured/not guaranteed		3	–	31/40	MHz
LPF 3dB cut-off frequency	F_{cut_LPF}	Tunable, assured/not guaranteed, relative to 5 MHz		15/11	–	31/40	MHz
IF (LPF&IFA) max gain	G_{MAX_IF}	–		–	63.5	–	dB
IF (LPF&IFA) min gain	G_{MIN_IF}	–		–	–0.5	–	dB
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	V_m	Note 4	Preset 1	–	200/470	–	mV
			Preset 2	–	400/980	–	
Output resistance	R_{out}	Analog differential output		–	200	–	Ohm
Group time delay ripple	ΔT_{GD}	Note 5	F_{IF} = 3–9MHz, F_{cut_LPF} = 18 MHz	–	<20	–	ns
			F_{IF} = 6–18MHz, F_{cut_LPF} = 25 MHz	–	<15	–	
Gain ripple	G_{IR}	LPF 3dB cut-off frequency excluded		–	1.5	–	dB
ADC							
Resolution	R_{ADC}	–		–	2	–	bit
ADC output signal level	V_{OH_ADC}	I_{LOAD} = 0mA/2mA	Preset 1	–	1.8/1.7	–	V
			Preset 2	–	2.4/2.3	–	
			Preset 3	–	2.7/2.6	–	
			Preset 4	–	V_{cc} /V_{cc} – 0.2	–	

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Synthesizer							
Reference frequency (TCXO)	F_{REF}	–		5	10/24.84	30	MHz
Reference input level	REF_{IN}	Sine or triangle wave		0.6	1	2	Vp-p
LO frequency range	F_{LO}	L1 band		1450	–	1650	MHz
		L2, L3, L5 band		1140	–	1300	
		S band		2280	–	2600	
VCO frequency range	F_{VCO}	VCO #1		2900	–	3300	MHz
		VCO #2		2280	–	2600	
VCO to PFD frequency integer-valued division ratio	N	Multiple of 2		96	–	1024	–
VCO to CLK frequency integer-valued division ratio	C	Multiple of 4		32	–	124	–
Reference frequency (TCXO) to PFD frequency integer-valued division ratio	R	–		1	–	15	–
LO phase noise	PN_{LO}	F_{PFD}= 24.84 MHz, F_{LO} = 1589.76 MHz	@100 kHz	–	–90	–	dBc/Hz
			@1 MHz	–	–115	–	
		F_{PFD}= 8.28 MHz, F_{LO} = 1233.72 MHz	@100 kHz	–	–88	–	
			@1 MHz	–	–117	–	
		F_{PFD}= 10 MHz, F_{LO} = 1590 MHz	@100 kHz	–	–89	–	
			@1 MHz	–	–116	–	
		F_{PFD}= 5 MHz, F_{LO} = 1235 MHz	@100 kHz	–	–89	–	
			@1 MHz	–	–118	–	
		F_{PFD}= 10 MHz, F_{LO} = 2480 MHz	@100 kHz	–	–81	–	
			@1 MHz	–	–110	–	
LO RMS jitter	J_{RMS}	Integrated BW = 25 MHz		–	3.5	–	ps
Clock frequency range (tunable)	F_{CLK}	F_{LO} = 1589.76 MHz		25.641	–	99.36	MHz
		F_{LO} = 1233.72 MHz		19.899	–	77.107	
		F_{LO} = 1590 MHz		25.645	–	99.375	
		F_{LO} = 1240 MHz or F_{LO} = 2480 MHz		20	–	77.5	
Peak-to-peak voltage at the differential clock outputs	V_{CLK}	R_{LOAD} = 200/0Ohm, F_{CLK} < 50 MHz, C_{load} < 10pF	Preset 1	–	230/460	–	mVp-p
			Preset 2	–	340/690	–	
			Preset 3	–	450/920	–	
			Preset 4	–	560/1130	–	
Output logic-level high at CMOS clock output	V_{OH_CLK}	F_{CLK} < 50 MHz, C_{load} < 5pF	Preset 1	–	1.8	–	V
			Preset 2	–	2.4	–	
			Preset 3	–	2.7	–	
			Preset 4	–	V_{CC}	–	
Output logic-level low at CMOS clock output	V_{OL_CLK}	–		0	–	0.2	V
PFD frequency range	F_{CMP}	–		1	10/24.84	30	MHz

Note 1: RFAGC = max gain, IFAGC gain > 30 dB
Note 2: RFAGC = min gain, IFAGC = min gain
Note 3: RFAGC = max gain, IFAGC = min gain
Note 4: RMS value measured. $V_{p\text{-}p\ sin} = V_{RMS} \times 2\sqrt{2}$; $V_{p\text{-}p\ noise} = V_{RMS} \times 6.6$
Note 5: Guaranteed by simulation

6. TYPICAL CHARACTERISTICS

Will be added for the next version.

7. APPLICATION NOTES

Some tricks or not obvious actions as well as configuration examples are described in this section.

IC configuration notes:

1) Both channel #1 and #2 must be enabled if at least one of them is used.
2) Both channel #3 and #4 must be enabled if at least one of them is used.
3) After switching from standby to active mode configuration file must be written again.

7.1. REFERENCE FREQUENCY (TCXO) CONFIGURATION AND START UP PROCEDURE

After power up NT1068 assumes feeding with 10MHz TCXO signal and wakes up in the active mode. PLLs are supposed to be locked after 1 ms and generally chip is ready for operation. During next 15 ms LPF calibration procedure is running in background mode and has no influence on channel filters. After completion a cut-off frequency correction code is applied to all channels automatically and NT1068 has following configuration:

- PLL "A" is set to L1 band and feeds channel#1 and channel#2 with LO = 1590 MHz
- PLL "B" is set to L2/L3/L5 band and feeds channel#3 and channel#4 with LO = 1235 MHz
- Channel#1 down converts lower sideband (i.e. L1 GPS/Galileo/BeiDou/QZSS)
- Channel#2 down converts upper sideband (i.e. L1 GLONASS)
- Channel#3 down converts upper sideband (i.e. L2 GLONASS)
- Channel#4 down converts lower sideband (i.e. L2 GPS/QZSS)
- All channels are set to analog differential output data interface, RF GC system in manual mode @ max gain, IF GC system in auto mode
- PLL "A" and PLL "B" tuning systems were executed
- LPF auto-calibration system was executed
- 53 MHz CLK of differential LVDS-like type is pushed out

IF another TCXO is used, some actions should be performed in order to make NT1068 perform properly. Execution sequence is important and described below:

- set Reg3 D[6–1] to desired TCXO frequency (select frequency range to which TCXO frequency belongs)
- perform PLL "A" and PLL "B" (if intended to use) reconfiguration according to sections 7.2 and 7.3 to get desired LO frequencies
- execute PLL "A" and PLL "B" (if intended to use) auto tuning procedure – Reg43 D[0] and Reg47 D[0] correspondingly
- execute LPF auto-calibration system – Reg4 D[0]

7.2. PLL "A"/ PLL "B" RECONFIGURATION

In order to reconfigure PLL following procedure is recommended:

- for operating in L2/L3/L5 or L1 band (Reg41/Reg45 D[2–1] is set to "00" or "01"):
  - using the formula: $F_{LO\_L} = \frac{N * F_{TCXO}}{R}$ choose N and R
  - write N value to Reg42/Reg46 D[7–0] + Reg43/Reg47 D[7]
  - write R value to Reg43/Reg47 D[6–3]
  - execute tuning procedure – Reg43/Reg47 D[0]
- for operating in "S for ch#1 + L2 for ch#2" mode (Reg41 D[2–1] is set to "11"):
  - using the formula: $F_{LO\_S} = \frac{2 * N * F_{TCXO}}{R}$ and $F_{LO\_L2} = \frac{N * F_{TCXO}}{R}$ choose common N and R for PLL "A"

  - write *N* value to Reg42 D[7–0] + Reg43 D[7]
  - write *R* value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]
- for operating in "L1 for ch#3 + L5 for ch#4" mode (Reg45 D[2–1] is set to "11"):
  - using the formula: $F_{LO\_L1} = \frac{N*F_{TCXO}}{R}$ and $F_{LO\_L5} = \frac{6*N*F_{TCXO}}{8*R}$ choose common *N* and *R* for PLL "B"
  - write *N* value to Reg46 D[7–0] + Reg47 D[7]
  - write *R* value to Reg47 D[6–3]
  - execute tuning procedure – Reg47 D[0]

PLLs need 1 ms to be locked.

In PLL "A" only mode (Reg2 D[1–0] is set to "01" or "10") it is recommended to set Reg41 D[2–1] to "00" or "01" and reconfigure PLL "A" according to the sequence given above if needed.

7.3. SINGLE LO SOURCE CONFIGURATION

In order to switch to single LO mode following actions are to perform:

- set Reg3 D[0] to "0" to feed all mixers from PLL "A"
- turn off PLL "B" by setting Reg45 D[0] to "0"
- for feeding channels with L2/L3/L5 or L1-band LO (Reg41 D[2–1] is set to "00" or "01"):
  - using the formula: $F_{LO\_L} = \frac{N*F_{TCXO}}{R}$ choose *N* and *R*
  - write *N* value to Reg42 D[7–0] + Reg43 D[7]
  - write *R* value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]
- for feeding all channels with S-band LO (Reg41 D[2–1] is set to "10"):
  - using the formula: $F_{LO\_S} = \frac{2*N*F_{TCXO}}{R}$ choose *N* and *R* for PLL "A"
  - write *N* value to Reg42 D[7–0] + Reg43 D[7]
  - write *R* value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]

7.4. RF AGC CONFIGURATION

RF GC system of NT1068 starts in the manual operation mode. You can change RF gain value manually by setting corresponding value with Reg17 D[7–4] for Channel#1 / Reg24 D[7–4] for Channel#2 / Reg31 D[7–4] for Channel#3 / Reg38 D[7–4] for Channel#4.

Actual RF power detector status is available at Reg9 D[5–4] in both manual and automatic modes. Reg9 D[5] indicates the crossing of upper threshold and Reg9 D[4] indicates the crossing of lower one. The thresholds are corresponding to the definite level of output power of input stage that's why they depend on RF gain value. The thresholds' values in section 4.4.2.4 are shown for max RF Gain settings (code "1111" is written to Reg17 D[7–4] for Channel#1 / Reg24 D[7–4] for Channel#2 / Reg31 D[7–4] for Channel#3 / Reg38 D[7–4] for Channel#4). To calculate the actual dBm-value of the threshold please use the equation:

$$TH_{ACT} = TH_{GTmax} + 19.5dB - GT_{SET},$$

where

TH_{ACT} – actual threshold value, dBm;
TH_{GTmax} – threshold value for max RF gain (shown in reg description table), dBm;
GT_{SET} – actual RF gain, chosen by settings, dB.

An upper threshold could be adjusted by Reg16 D[6–4] for Channel#1 / Reg23 D[6–4] for Channel#2 / Reg30 D[6–4] for Channel#3 / Reg37 D[6–4] for Channel#4. A lower threshold could be adjusted by Reg16 D[2–0] for Channel#1 / Reg23 D[2–0] for Channel#2 / Reg30 D[2–0] for Channel#3 / Reg37 D[2–0] for Channel#4. Power values shown in registers description table are calculated with respect to input signal power. The upper threshold should always be higher than lower. Also it is strongly recommended to set dBm-value of upper threshold at least 3dB higher than lower threshold to guarantee stability of RF AGC loop.

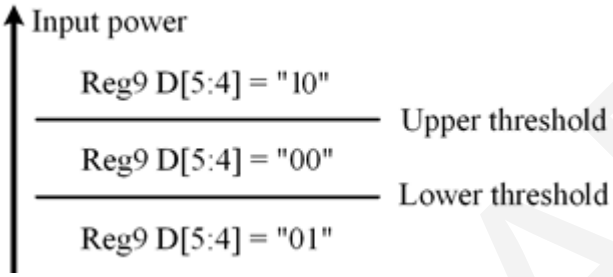


Figure 7.1: RF AGC power detector status operation logic

The RF AGC thresholds can be changed in order to improve RF channel linearity by decreasing dBm value of both thresholds (IM3 will increase since each block will operate with weaker input signal) or to improve RF channel noise figure by increasing thresholds' dBm value (noise of channel blocks will be more suppressed by higher gain of input amplifier and SNR of the receiver will be improved).
To enable automatic mode the Reg15 D[4] for Channel#1 / Reg22 D[4] for Channel#2 / Reg29 D[4] for Channel#3 / Reg36 D[4] for Channel#4 should be switched to “1”. While automatic mode enabled, the RF AGC system will adjust the RF gain to keep its output power between RF AGC thresholds.
The status of RF gain control register is available at Reg9 D[3–0].

7.5. IF AGC THRESHOLD CONFIGURATION

If 400mV (w.r.t. sine wave signal) option is chosen for output peak-to peak voltage (Reg15 D[6] for Channel#1 / Reg22 D[6] for Channel#2 / Reg29 D[6] for Channel#3 / Reg36 D[6] for Channel#4) it is recommended not to solder terminating 200 Ohm resistor and to write appropriate values (“0”) to D[5] of the same registers. It will result in better linearity performance.

7.6. LPF CALIBRATION

LPF automated calibration procedure is intended to compensate influence of temperature dependence and technological scatter on LPF characteristics. It automatically starts at power up, however it is recommended to manually run it if operation temperature significantly differs from typical or if TCXO frequency was changed. LPF autocalibration system status is available in Reg4 D[1]. LPF autocalibration procedure takes about 15ms. In Reg14 D[6–0] for channel#1, Reg21 D[6–0] for channel#2, Reg28 D[6–0] for channel#3 and Reg35 D[6–0] for channel#4 guaranteed range of LPF cut-off frequency is described for typical conditions. On marginal samples autocalibration system will compensate offset either in low-frequency range or in high-frequency range. After autocalibration you will get 3dB attenuation at the selected setting of guaranteed range for any chip in the specified temperature range.

7.7. 2-BIT ADC CONFIGURATION

After power up NT1068 is preconfigured to analog differential output data interface. However, there is an option to set up 2-bit ADC outputs in Reg15 D[0] for Channel#1 / Reg22 D[0] for

Channel#2 / Reg29 D[0] for Channel#3 / Reg36 D[0] for Channel#4. 2-bit ADCs are able to operate in one of three modes:

- clocked by rising edge;
- clocked by falling edge;
- asynchronous.

These modes can be set up in Reg19 D[3–2] for Channel#1 / Reg26 D[3–2] for Channel#2 / Reg33 D[3–2] for Channel#3 / Reg40 D[3–2] for Channel#4. For ADCs sampling frequency information, please, refer to section 7.8. In "asynchronous" mode 2-bit ADCs act as voltage level comparators so no any clocking applied. For example, this mode may be use full if several NT1068s should operate simultaneously pushing out digitized data that can be synchronized with single clock on correlator and processor side.

7.8. CLK FREQUENCY CONFIGURATION

CLK signal is intended for clocking all 2-bit ADCs as well as clocking external correlator engine. It is generated from LO frequency either from PLL "A" or PLL "B". CLK source and frequency can be customized by procedure:

- choose CLK source by setting appropriate value to Reg12 D[5]
- if operating in L2/L3/L5 or L1 band (Reg3 D[0] is set to "0" or "1" and Reg41/Reg45 D[2–1] is set to "00" or "01"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L}}{2*C}$ choose C
  - write C value to Reg11 D[4–0]
- if operating in S+L2 bands (Reg3 D[0] is set to "1" and Reg41 D[2–1] is set to "11"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L2}}{2*C}$ and $F_{CLK} = \frac{F_{LO\_S}}{4*C}$ choose common C
  - write C value to Reg11 D[4–0]
- if operating in L1+L5 bands (Reg3 D[0] is set to "1" and Reg45 D[2–1] is set to "11"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L1}}{2*C}$ and $F_{CLK} = \frac{2*F_{LO\_L5}}{3*C}$ choose common C
  - write C value to Reg11 D[4–0]
- if operating in S band (Reg3 D[0] is set to "0" and Reg41 D[2–1] is set to "10"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_S}}{4*C}$ choose C
  - write C value to Reg11 D[4–0]

If Reg3 D[0] is set to "0" PLL "B" will be available only for generating CLK frequency.

If CLK signal is not needed for external application, CLK output can be disabled by setting Reg12 D[6] to "1". In this case sampling frequency will be available only for internal 2-bit ADCs.

7.9. CLK OUTPUT TYPE USAGE

Although CMOS output is available for usage it is recommended to select differential LVDS-like CLK output. It is related to appearing of interferences at the LNA#_IN pins and then down converting to IF band. These interferences are caused by CLK signal harmonics and allocated frequencies can be calculated as $F_{jam} = N * F_{CLK}, N = 1,2,3,4 \ldots$

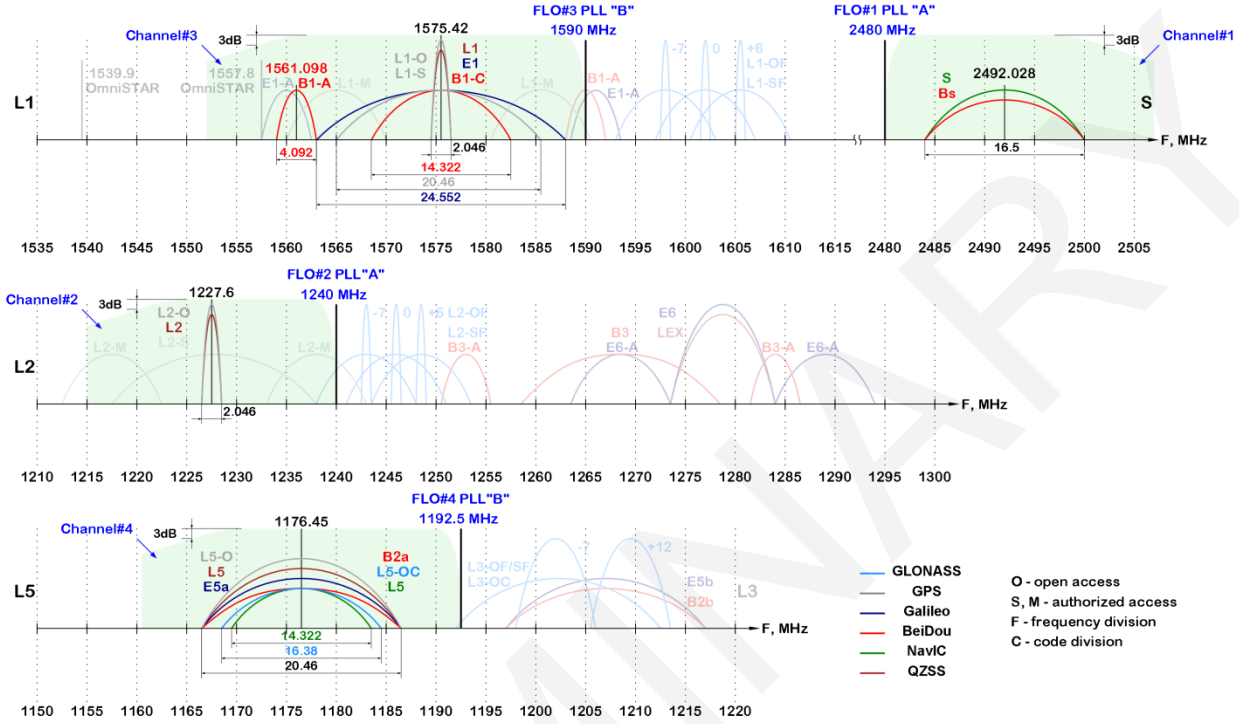
7.10. TEMPERATURE MEASUREMENT PROCEDURE

Two modes of temperature modes are available: single and continuous (Reg5 D[1]). In single mode the measurement is done once upon request to Reg5 D[0] by setting "1" and result will be stored in Reg7 D[1–0] + Reg8 D[7–0] after procedure is finished (auto reset to "0" in Reg5 D[0] indicates this) until next execution. One temperature measurement procedure time is up to 17 ms.

To enter in continuous mode set Reg5 D[1] to “1” first then execute with Reg5 D[0]. In this case embedded temperature sensor periodically runs the measurement procedure and only the latest result is stored in Reg7 D[1–0] + Reg8 D[7–0]. In order to stop continuous execution Reg5 D[1] should be set to “0”.

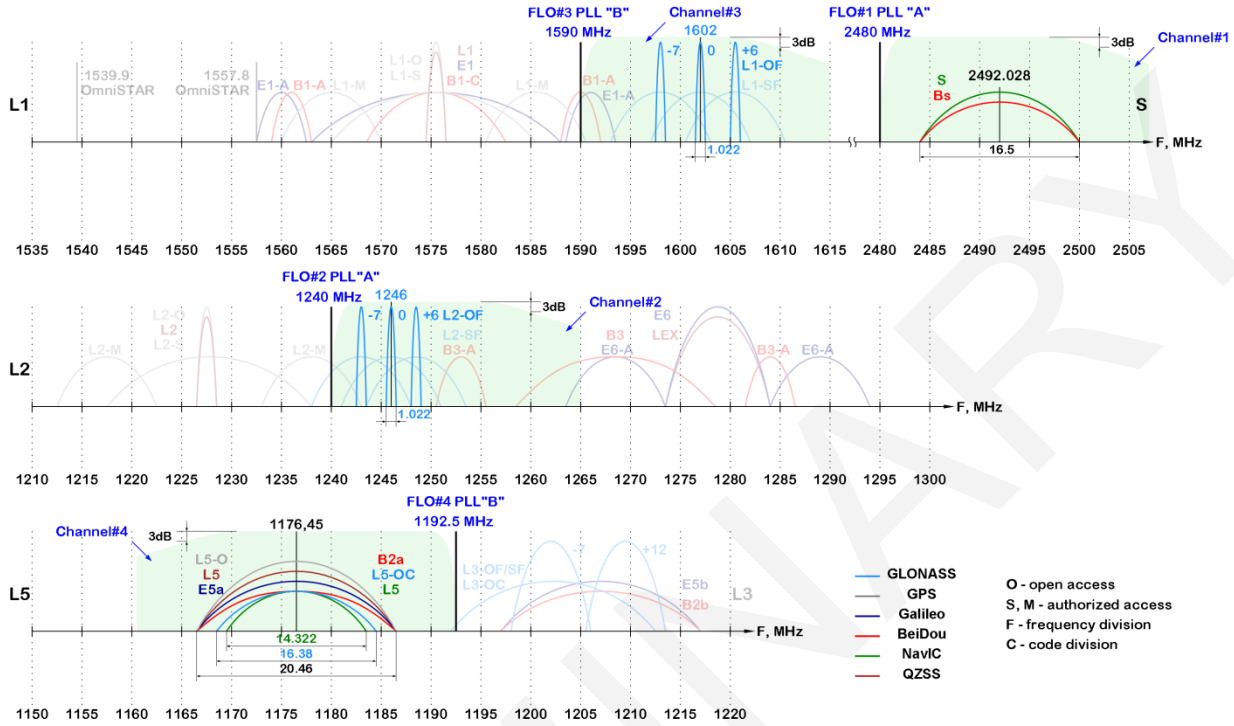
7.11. OPERATION EXAMPLES

7.11.1. CONFIGURATION SET #1



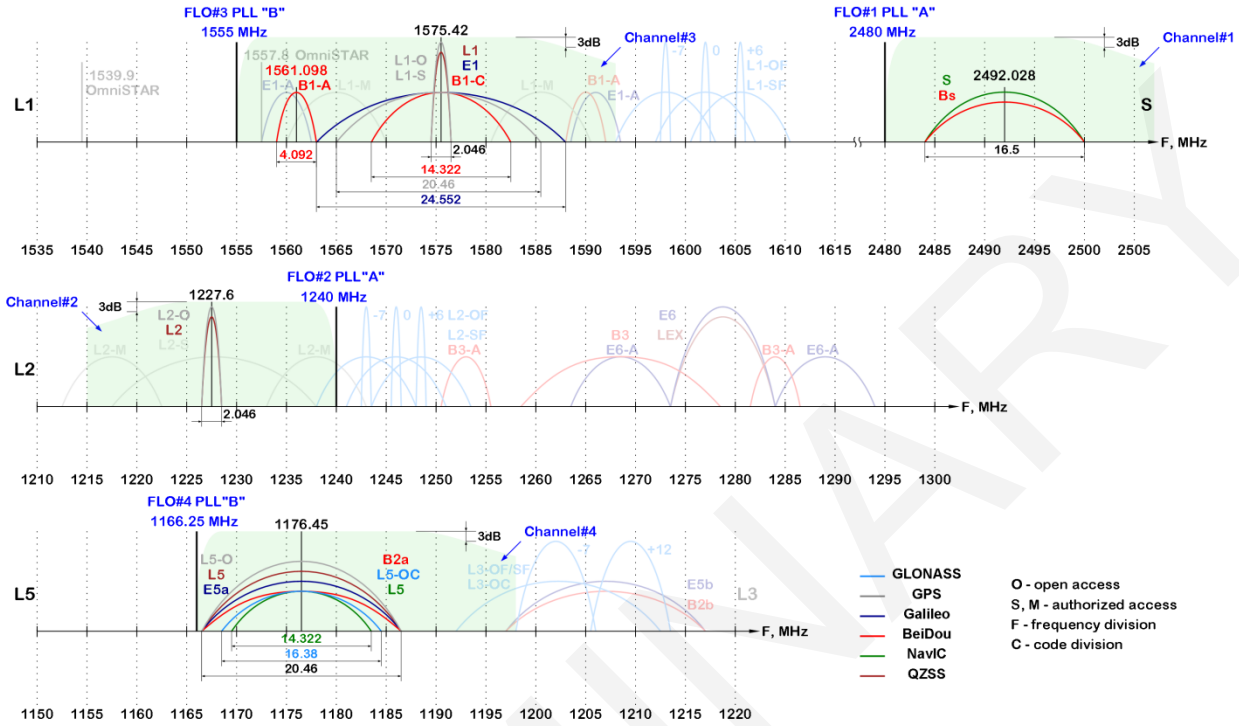
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	68.9 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Lower sideband (GPS L2, QZSS L2)
Ch#3 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	33 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	2480 MHz
F_{LO}#2 PLL “A”	1240 MHz
F_{LO}#3 PLL “B”	1590 MHz
F_{LO}#4 PLL “B”	1192.5 MHz

7.11.2. CONFIGURATION SET #2



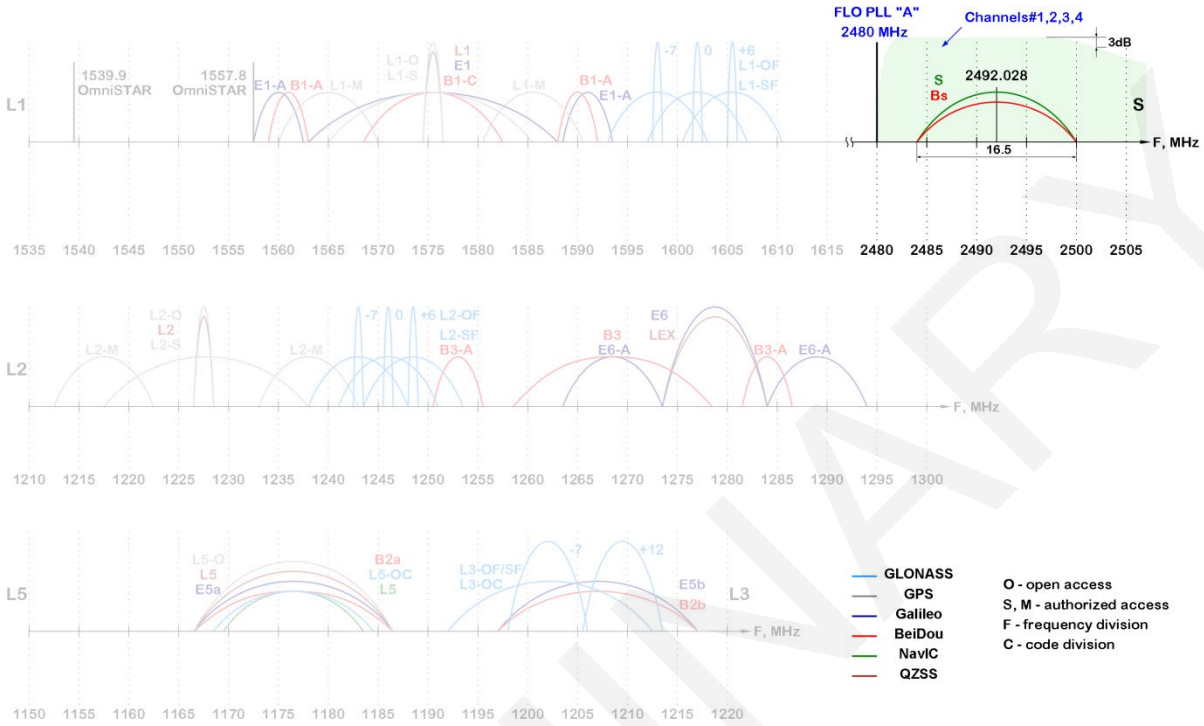
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	62 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Upper sideband (GLONASS L2)
Ch#3 GNSS	Upper sideband (GLONASS L1)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	20 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	2480 MHz
F_{LO}#2 PLL “A”	1240 MHz
F_{LO}#3 PLL “B”	1590 MHz
F_{LO}#4 PLL “B”	1192.5 MHz

7.11.3. CONFIGURATION SET #3



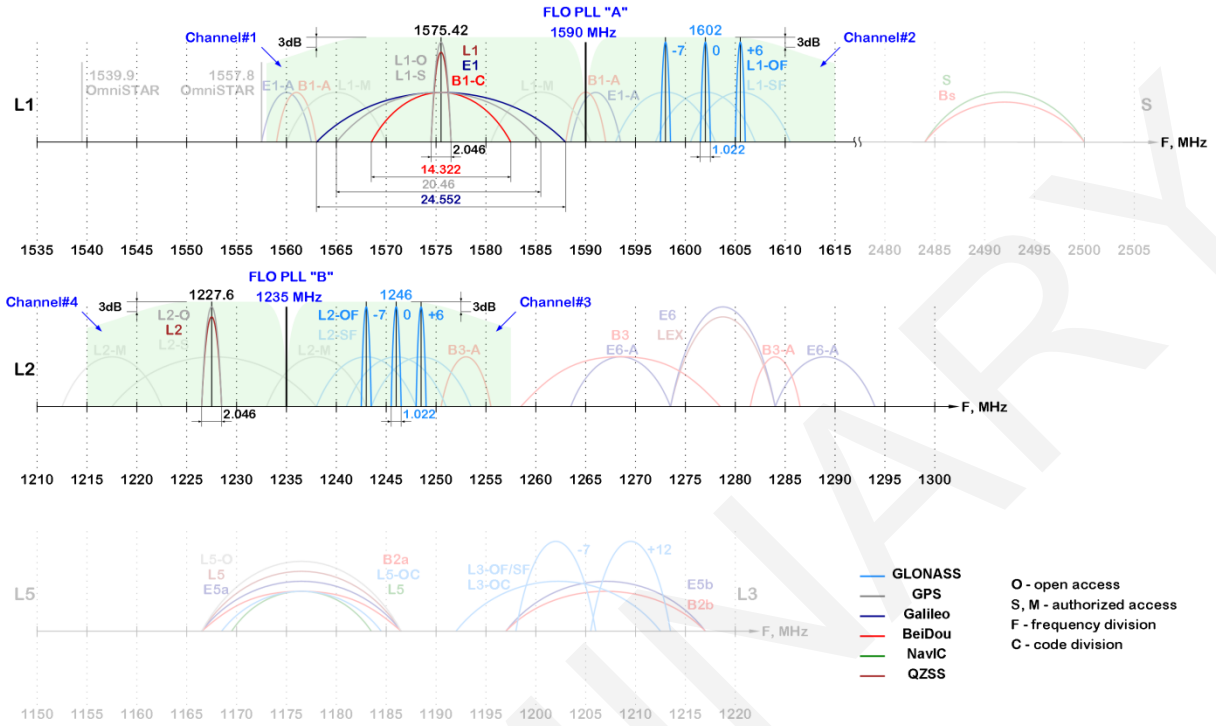
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	68.9 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Lower sideband (GPS L2, QZSS L2)
Ch#3 GNSS	Upper sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1)
Ch#4 GNSS	Upper sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	33 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	2480 MHz
F_{LO}#2 PLL “A”	1240 MHz
F_{LO}#3 PLL “B”	1555 MHz
F_{LO}#4 PLL “B”	1166.25 MHz

7.11.4. CONFIGURATION SET #4



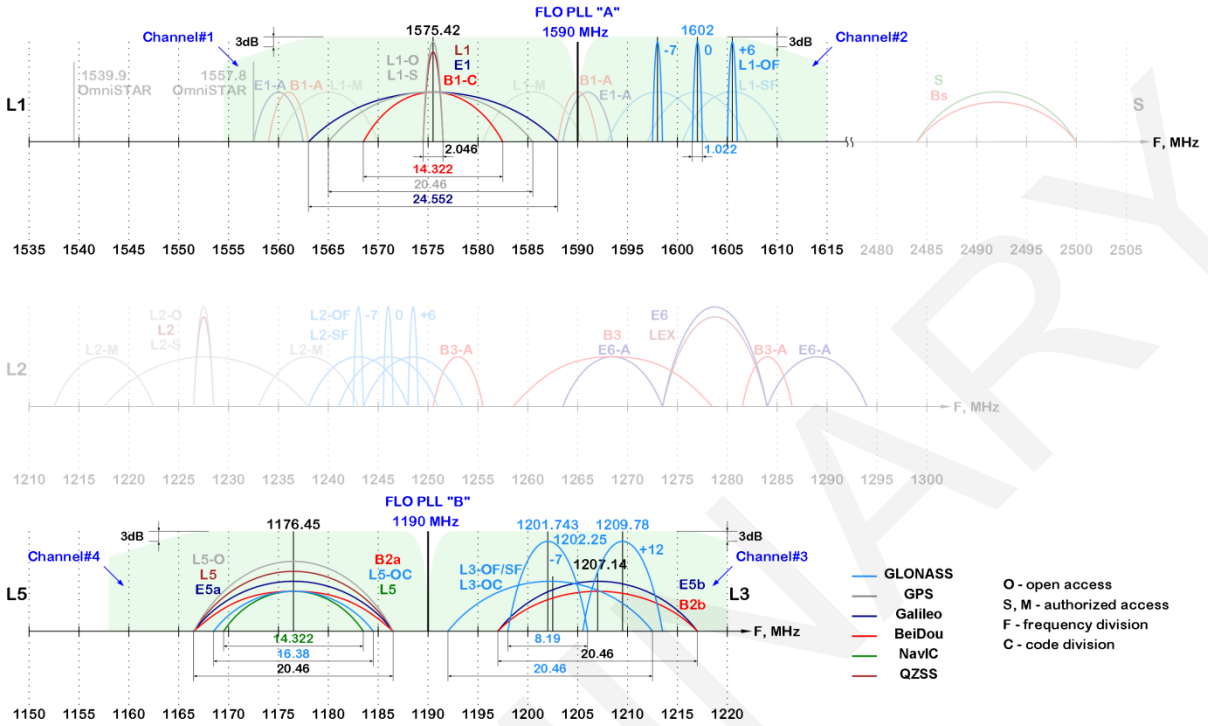
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for all channels
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	47.7 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#3 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#4 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	22 MHz
Ch#3 IF passband	22 MHz
Ch#4 IF passband	22 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	2480 MHz

7.11.5. CONFIGURATION SET #5



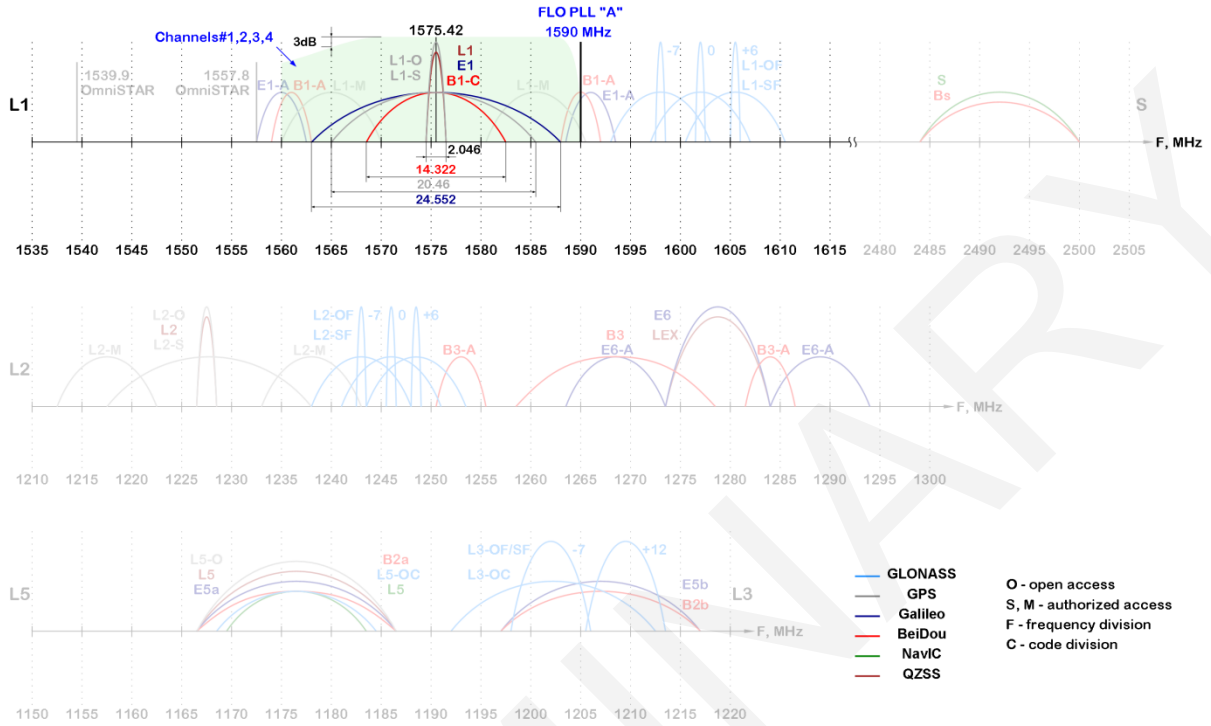
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	53 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.56V
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Upper sideband (GLONASS L1)
Ch#3 GNSS	Upper sideband (GLONASS L2)
Ch#4 GNSS	Lower sideband (GPS L2, QZSS L2)
Ch#1 IF passband	27 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	17.5 MHz
Ch#4 IF passband	15 MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1235 MHz

7.11.6. CONFIGURATION SET #6



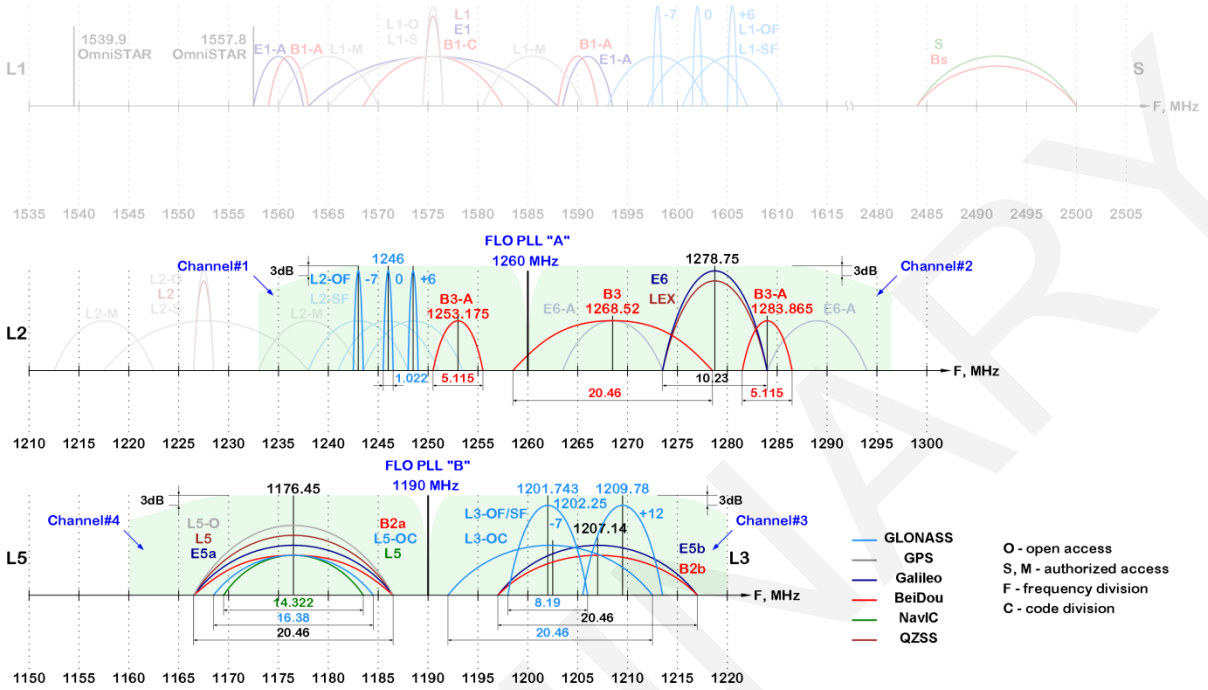
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	61.2 MHz
CLK output type	CMOS
CLK output amplitude	Ext. (VCC)
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Upper sideband (GLONASS L1)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30.5 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	30 MHz
Ch#4 IF passband	27 MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1190 MHz

7.11.7. CONFIGURATION SET #7



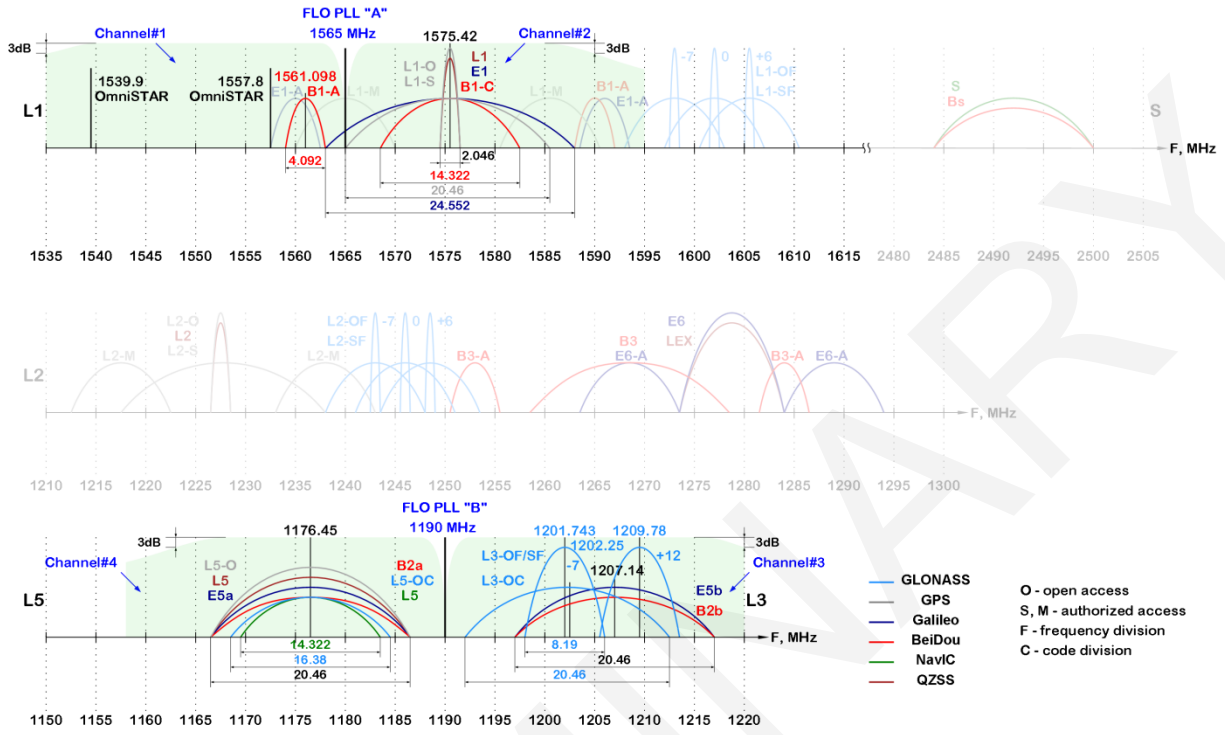
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for all channels
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	53 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#3 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#4 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#1 IF passband	25 MHz
Ch#2 IF passband	25 MHz
Ch#3 IF passband	25 MHz
Ch#4 IF passband	25 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	1590 MHz

7.11.8. CONFIGURATION SET #8



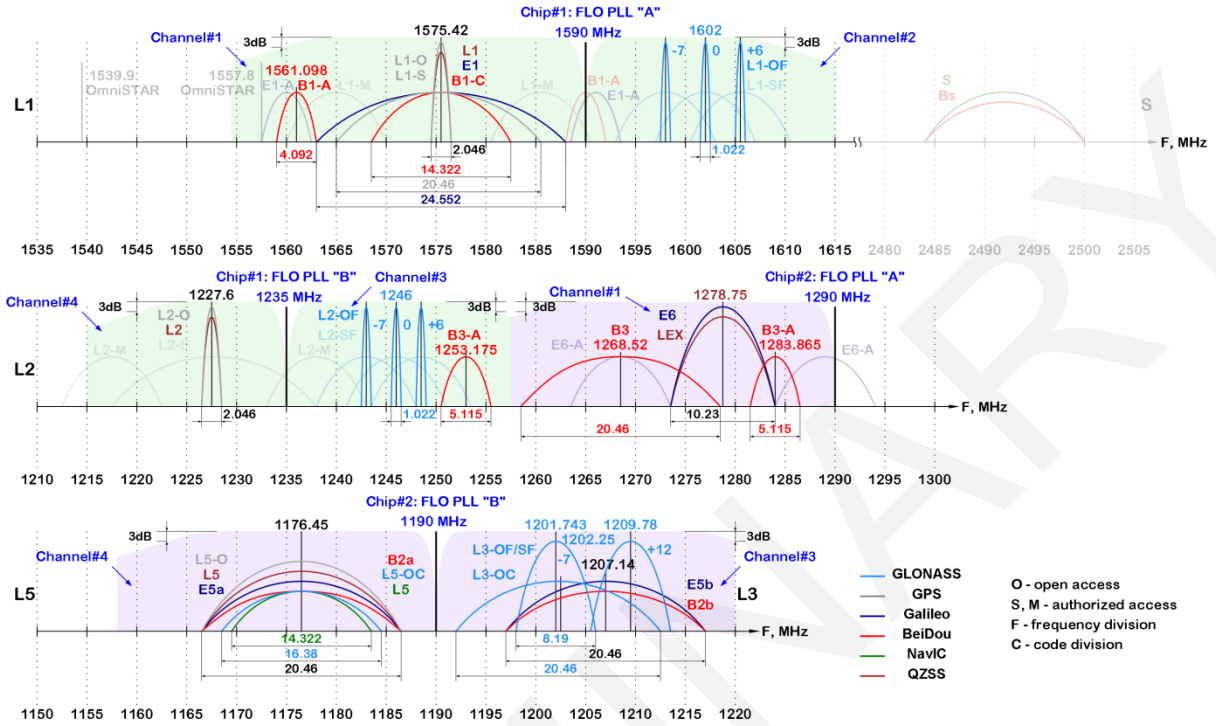
General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	70 MHz
CLK output type	Differential LVDS-like
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Lower sideband (GLONASS L2, BeiDou B3-A)
Ch#2 GNSS	Upper sideband (BeiDou B3, Galileo E6, QZSS LEX)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	32 MHz
Ch#3 IF passband	28 MHz
Ch#4 IF passband	25 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	1260 MHz
F_{LO} PLL “B”	1190 MHz

7.11.9. CONFIGURATION SET #9



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	97.812 MHz
CLK output type	CMOS
CLK output amplitude	Ext.
Channel settings:	
Ch#1 GNSS	Lower sideband (OmniStar 1557.8MHz, OmniStar 1539.9MHz, BeiDou B1-A)
Ch#2 GNSS	Upper sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30 MHz
Ch#2 IF passband	25 MHz
Ch#3 IF passband	30 MHz
Ch#4 IF passband	28 MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1565 MHz
F_{LO} PLL “B”	1190 MHz

7.11.10. CONFIGURATION SET #10



General settings:	Chip#1	Chip#2
Reference frequency (TCXO)	10 MHz	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
Channel settings:		
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1)	Lower sideband (BeiDou B3, Galileo E6, QZSS LEX)
Ch#2 GNSS	Upper sideband (GLONASS L1)	–
Ch#3 GNSS	Upper sideband (GLONASS L2, BeiDou B3-A)	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L2, QZSS L2)	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30.5 MHz	31 MHz
Ch#2 IF passband	20 MHz	–
Ch#3 IF passband	21 MHz	30 MHz
Ch#4 IF passband	15 MHz	27 MHz
Output data interface	2-bit ADC	2-bit ADC
GC mode	RF manual + IF auto	RF manual + IF auto
IF AGC threshold	30%	30%
ADC output logic-level high	Ext. (VCC)	Ext. (VCC)
ADC type	Clocked by rising edge	Clocked by rising edge
PLL settings:		
F_{LO} PLL “A”	1590 MHz	1290 MHz
F_{LO} PLL “B”	1235 MHz	1190 MHz

7.12. PCB LAYOUT RECOMMENDATIONS

Will be added for the next version.

8. PACKAGE INFORMATION

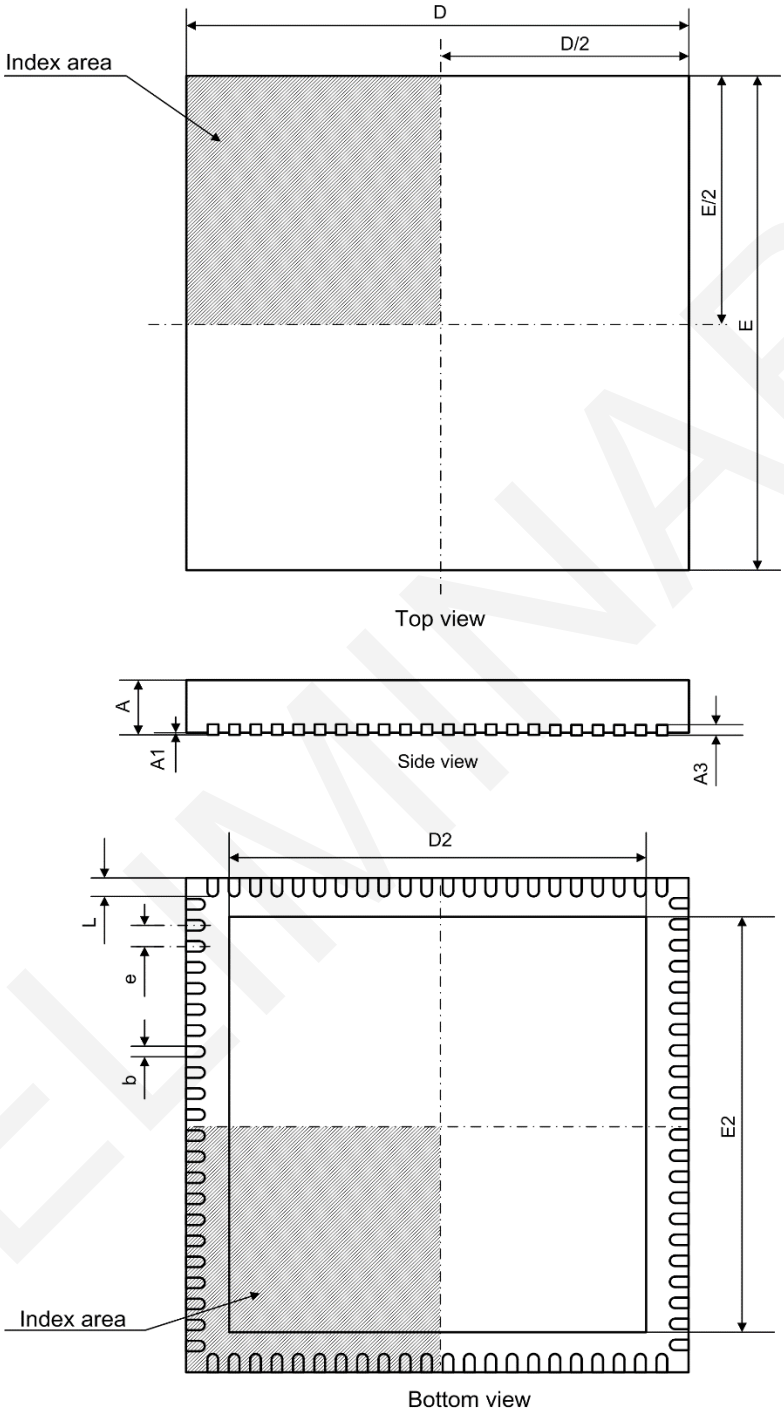


Figure 8.1: Package QFN88 10×10[1]

Table 8.1: Package QFN88 10×10 dimensions[1]

Unit	A	A1	A3	b	D	D2	E	E2	e	L
min, mm	0.80	0.00		0.15	9.90	8.05	9.90	8.05		0.30
typ., mm	0.85	0.02	0.20	0.20	10.00	8.20	10.00	8.20	0.4	0.40
max, mm	0.90	0.05		0.25	10.10	8.35	10.10	8.35		0.50

Note 1: Package drawing and dimensions are for reference only. Actual values are compliant to JEDEC standard outlines MO–220.

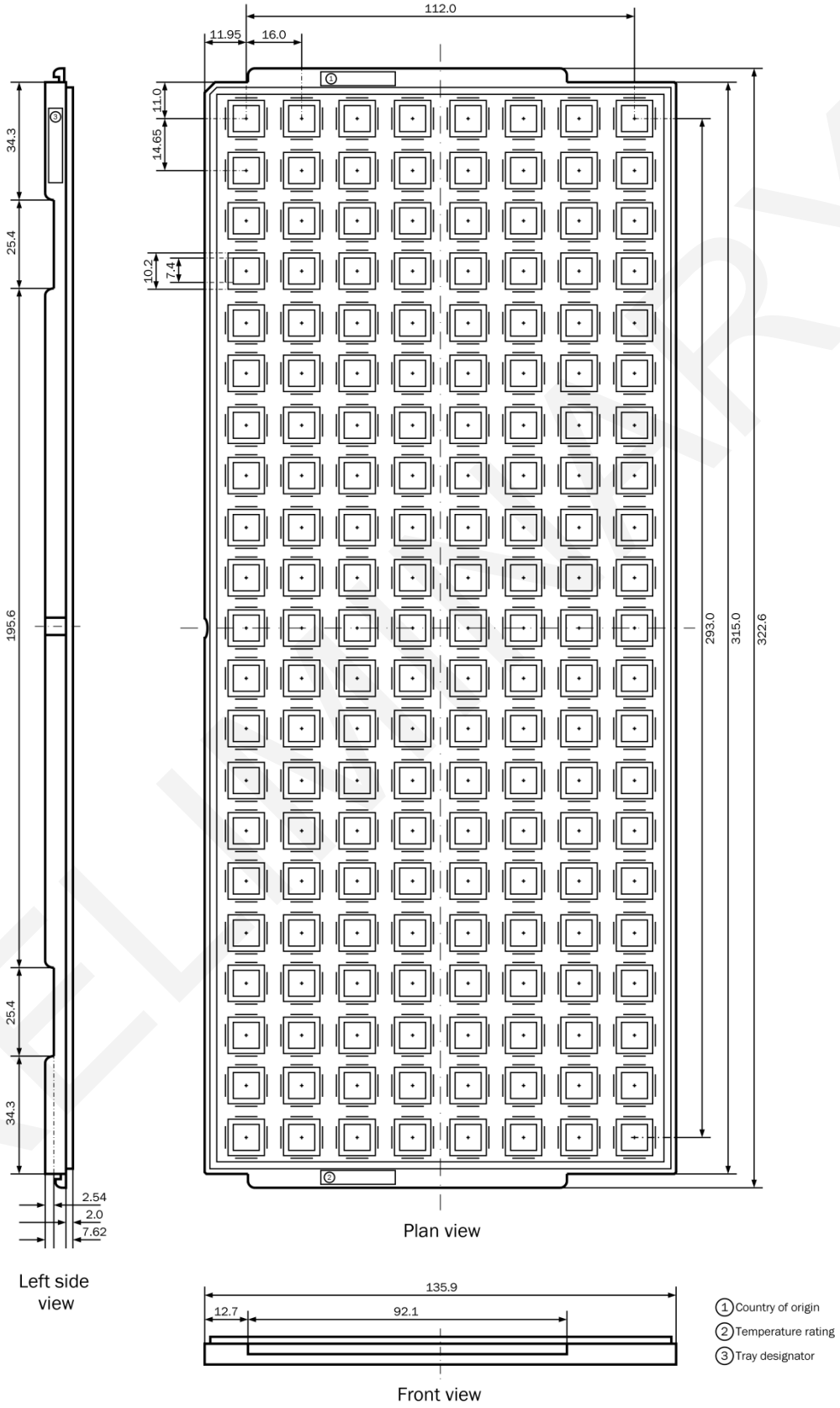


Figure 8.2: Matrix tray 8×12 for QFN88 10×10 [2]

Note 2: All dimensions are in mm. Tray drawing and dimensions are for reference only. Actual values are compliant to JEDEC standard outlines CO–034.

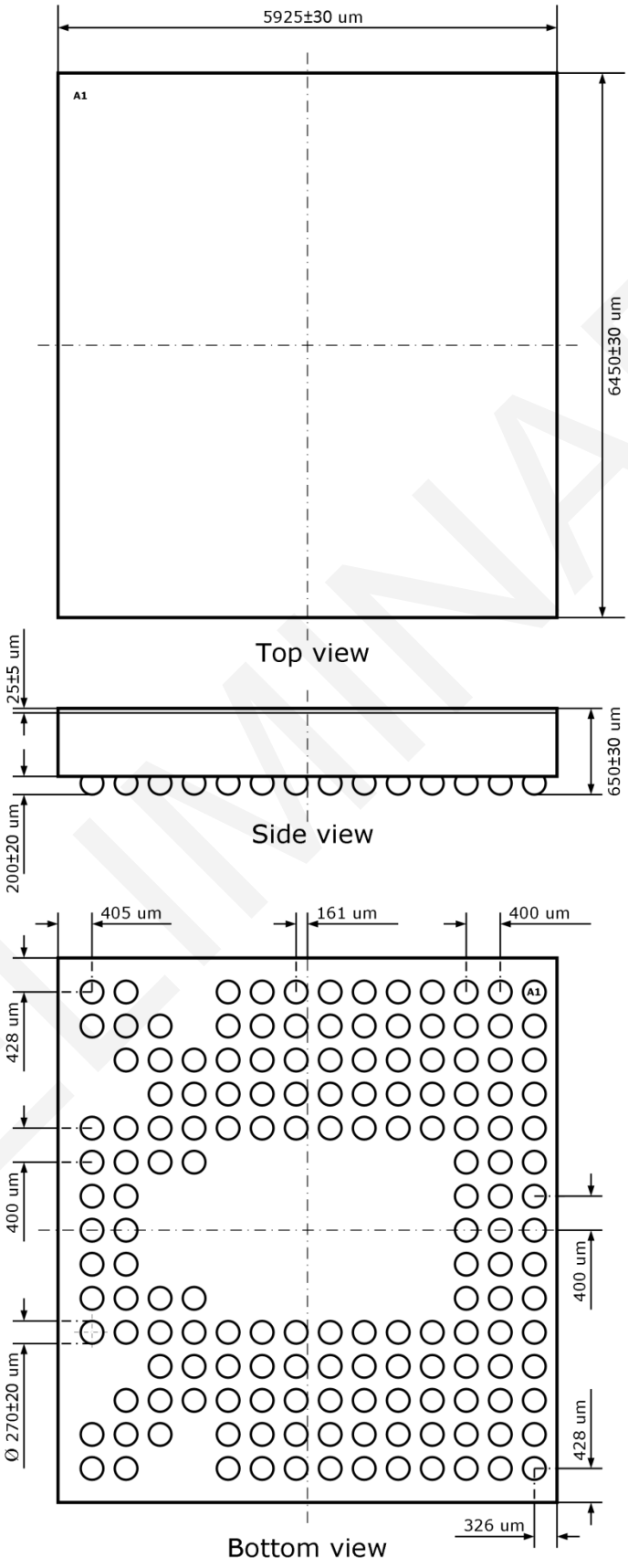


Figure 8.3: WLCSP drawing