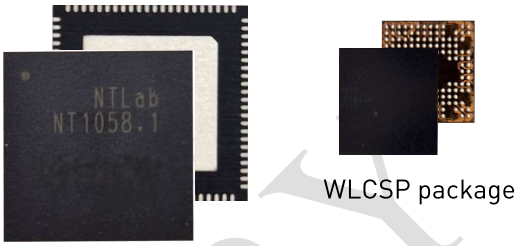
NT1058.AR
GNSS BASEBAND PROCESSOR

NT1058.AR is a computing system on a crystal, which include digital Baseband Processor, HAS signal demodulation IP block, IP cryptographic block for OSNMA implementation and 128-channels hardware correlator for tracking and primary processing of digital signals of Galileo (E1, E5b, E5a, E6, E5 AltBOC), GPS (L1, L2, L5), GLONASS (G1, G2), BeiDou (B1, B2) GNSS constellations.

Package preliminary view



WLCSP package

12x12mm QFN108

(Appearance may differ from the view above (in color, print, dimensions, PINs)

FEATURES

CORE
- 32-bit RISC-V general purpose processor
- Two coprocessors for implementation HAS and OSNMA demodulation
- Floating point coprocessor
- Frequency up to 250 MHz for central processing unit and up to 125 MHz for digital processing units
- 6TE architecture ARM instruction set

ON CHIP RAM
- 2 MB static RAM for general CPU
- 64 KB static RAM for each HAS and OSNMA uCPUs
- 64 KB static RAM for correlators
- 32 KB static RAM for battery backup
- 64 KB static RAM for recorder and channel search accelerator
- Direct access to memory from DMA controller

POWER MANAGEMET
- 1.2V ±10% and 1.8V ±10% supply voltage
- POR
- LDO 1.0V for clock power and back-up memory

ADDING BIULT-IN ANALOG COMPONENTS
- 8x 2-bit ADC

CLOCK MANAGEMET
- 32,768 KHz clock oscillator
- 6 MHz RC oscillator (clock source on reset)
- 50-800MHz phase-locked loop

EVENT COMPONENTS
- 2 event mark
- 2 event former

DSP ENGINE
- Up to 128 BPSK correlators
- 32 CBOC/ AltBOC correlators
- 128-channels search accelerator
- Additional code generators: 16 RAM-based 2-bits pseudorange code and 16 P-Code generators
- Input complex bandwidth – up to 125MHz
- 128 kS recoder
- Interference detection and mitigation
- Timescale PPS
- Hardware FFT accelerator

INTERFACES AND PERIPHERIALS
- Data interfaces: I²C, UART, SPI
- JTAG interface for debug and testing
- General purpose timer
- Interrupt controller
- General purpose IO ports
- Direct memory access (DMA) controller
- Real time counter

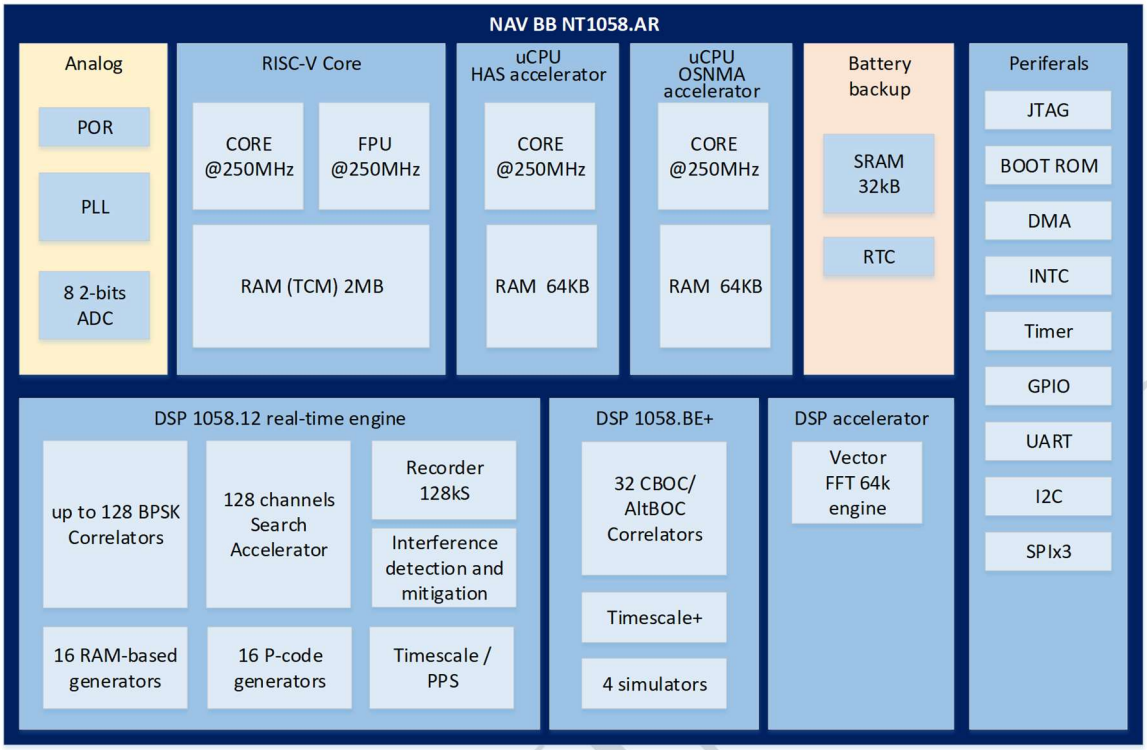
APPLICATION
- GNSS based positioning systems
- GNSS based goniometric systems
- In-vehicle navigation systems
- GNSS based driverless car systems
- Professional drones
- Aviation navigation systems
- Noise-proof time servers

VYTIS-AR

This project has received funding from the European Union Agency for the Space Programme **EUSPA/GRANT/02/2022**

EUSPA European Union Agency for the Space Programme

PRELIMINARY BLOCK DIAGRAM



PRELIMINARY MAIN OPERATING CHARACTERISTICS

- Supply voltage 1.2V ±10% and 1.8V ±10%
- Battery supply voltage 1.0 ... 1.6V (1.4V typ)
- Temperature range T_a =–40 ÷ 85°C
- CPU operating clock frequency up to 250 MHz
- DSP operating clock frequency up to 125 MHz
- ADC
  - DC input signal 1.4 ... 1.7V (1.55V typ)
  - Comparison threshold 62.22 .. 217.22 mV
  - Input Amplitude ~40 ... ~150 mV
  - Sampling rate 50 ... 100 PSPS
  - Clock frequency 50 ... 125 MHz
  - Bandwidth 50 ... 125 MHz
  - Resolution 2 bit
  -
- Crystal oscillator
  - Quartz frequency 32.768 KHz
  - Output signal duty cycle (50±10) %
- PLL
  - VCO frequency 400 ... 800 MHz
  - Output frequency 50 ... 800 MHz
  - LO duty cycle (50±10) %
  - Phase noise -96.2 dBc/Hz (F_{LO} = 400MHz at 1MHz)
    92.5 dBc/Hz (F_{LO} = 800MHz at 1MHz)
  - Reference frequency 4 ... 20 MHz (5 MHz typ)
  - Reference clock duty cycle (50±10) %
  - Lock time up to 14 µs (9 µs typ)
  - Lock detector accuracy 15 ... 27 ns (20 ns typ)

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