2-Channel GPS/GLONASS/Galileo/BeiDou/NavIC/GAGAN/QZSS L1/L2/L3/L5 band RF Front-End IC

1. OVERVIEW

NT1062 is a 2-channel RF Front-End IC intended for the reception of GNSS (GPS, GLONASS, Galileo, BeiDou, NavIC, GAGAN, QZSS) signals like L1, L2, L3, L5, E1, E5a, E5b, E6, B1, B2, B3 and also satellite-based augmentation systems like OmniSTAR and SBAS in various combinations. It makes possible to benefit from all the advantages of acquiring multiple system with single chip. Two real channels with image rejection are designed with single conversion low-IF architecture. External active antenna can be connected to RF input that is common for two channels. As an option two separate RF inputs can be used for operating with external passive antennas. Each channel setting, including output signal frequency bandwidth, AGC options, mirror channel suppression option, etc., can be set for each channel individually. NT1062 includes two fully independent frequency synthesizers that have the common reference (TCXO) input making LO signals coherent in terms of frequency.

2. FEATURES

- Single conversion super heterodyne architecture
- 2 independent customizable real channels with image rejection
- 2 PLLs with fully integrated VCOs and autotuning system
- Internal 1-to-2 RF splitter and 2 separate RF inputs
- Active antenna detection system including supply and short-protection circuits
- IF LPF with tunable signal bandwidth
- Analog differential outputs or 2-bit ADC outputs
- IF AGC system or manually programmable gain
- Power management unit for supplying of internal blocks and external components like LNAs, active antenna and TCXO
- Low power consumption
- Clock output for external correlator with programmable frequency
- 3-wire SPI interface with user friendly registers map
- Three form-factors: 5mm×5mm QFN32 / 2.7mm×2.7mm WLCSP / 2.7mm×2.7mm bare die

3. APPLICATIONS

- Cellular consumer electronics
- GNSS based positioning systems
- GNSS based goniometrical systems

4. DESCRIPTION

4.1. BLOCK DIAGRAM

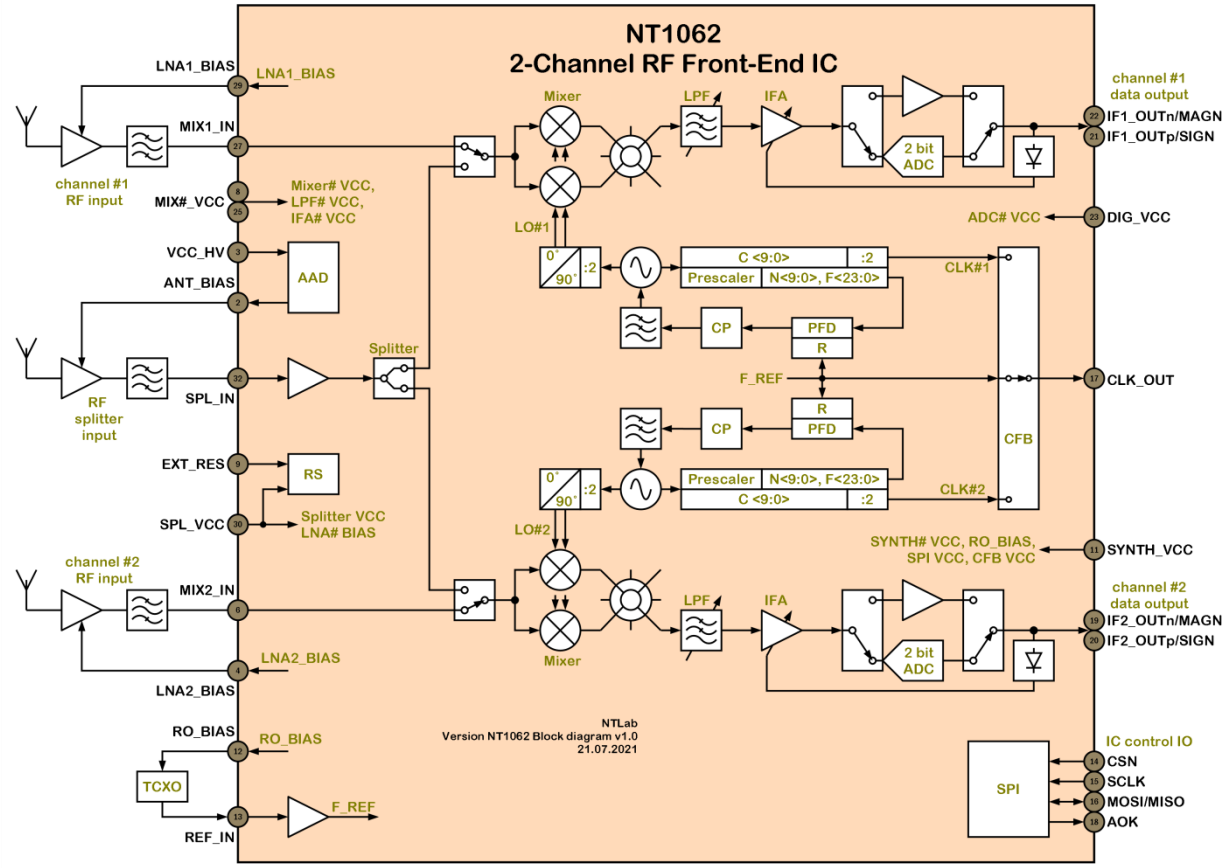


Figure 4.1: NT1062 Block diagram

4.2. APPLICATION SCHEMATIC

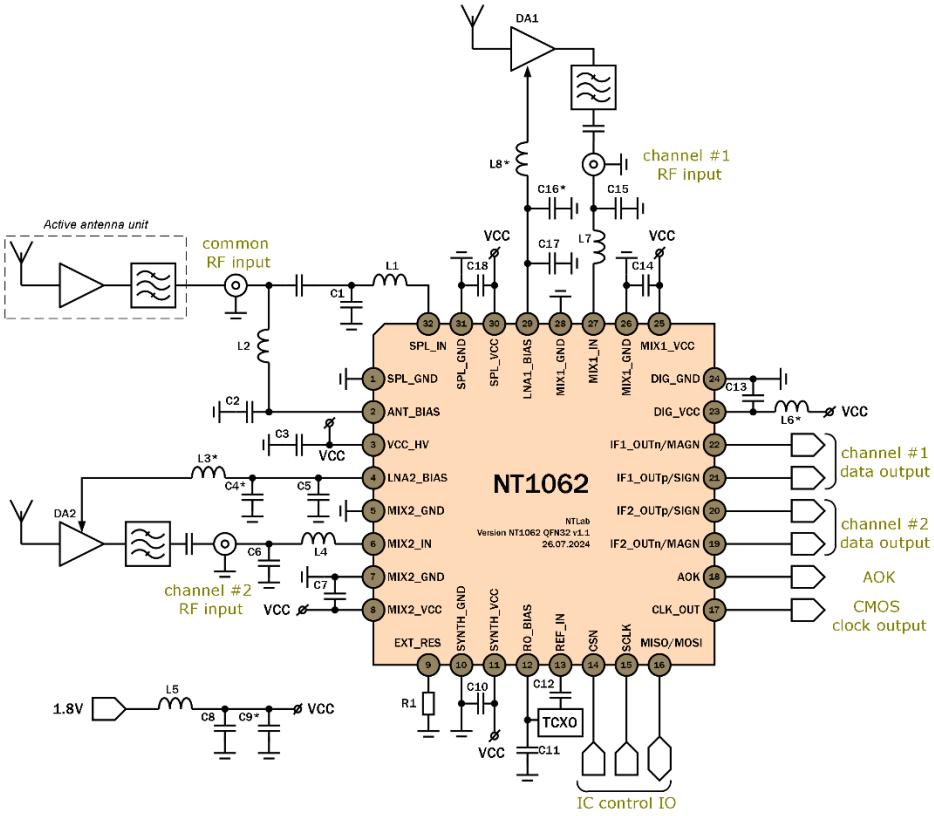


Figure 4.2: NT1062 QFN32 full application schematic (one supply voltage domain)

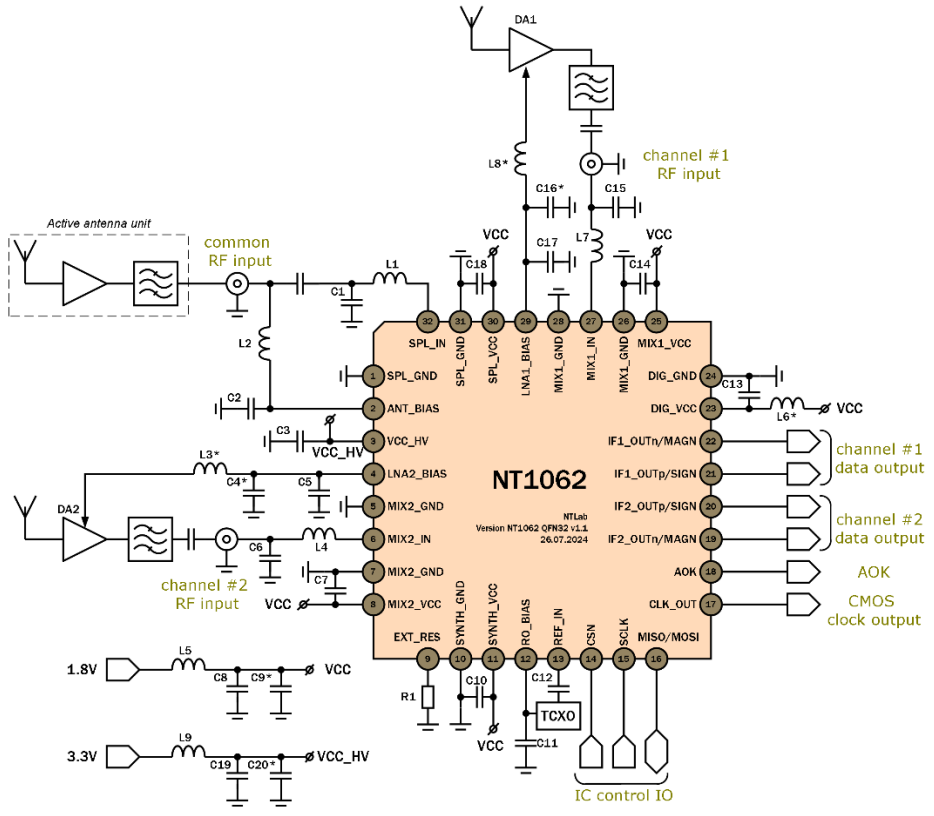


Figure 4.3: NT1062 QFN32 full application schematic (two supply voltage domains)

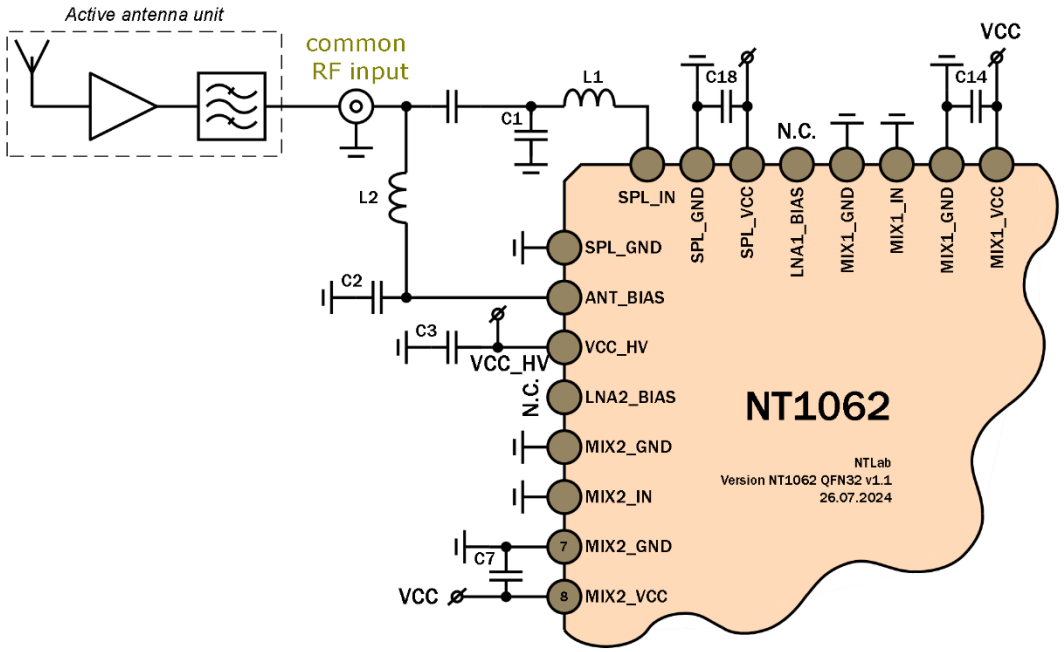


Figure 4.4: NT1062 QFN32 specific application schematic (common RF input)

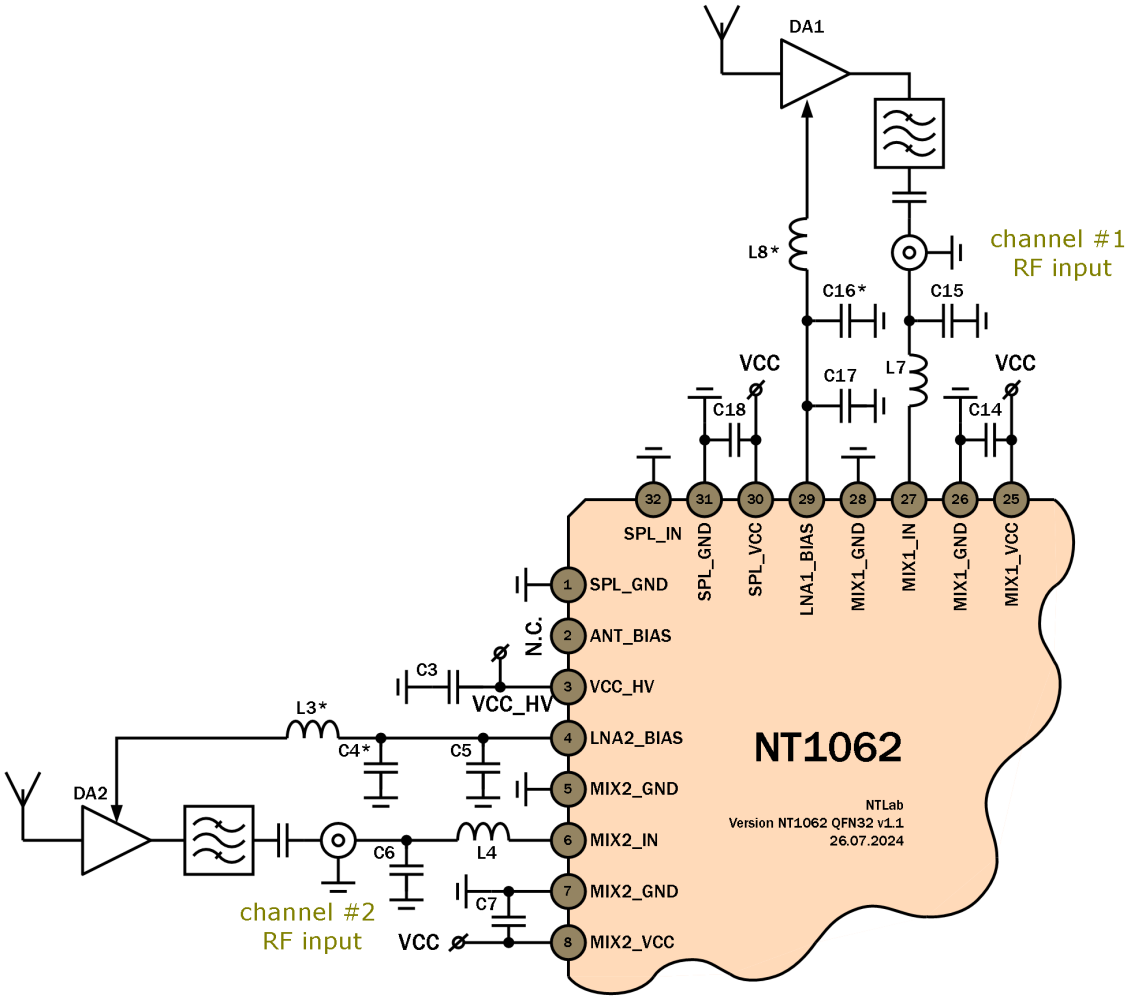


Figure 4.5: NT1062 QFN32 specific application schematic (separate RF inputs)

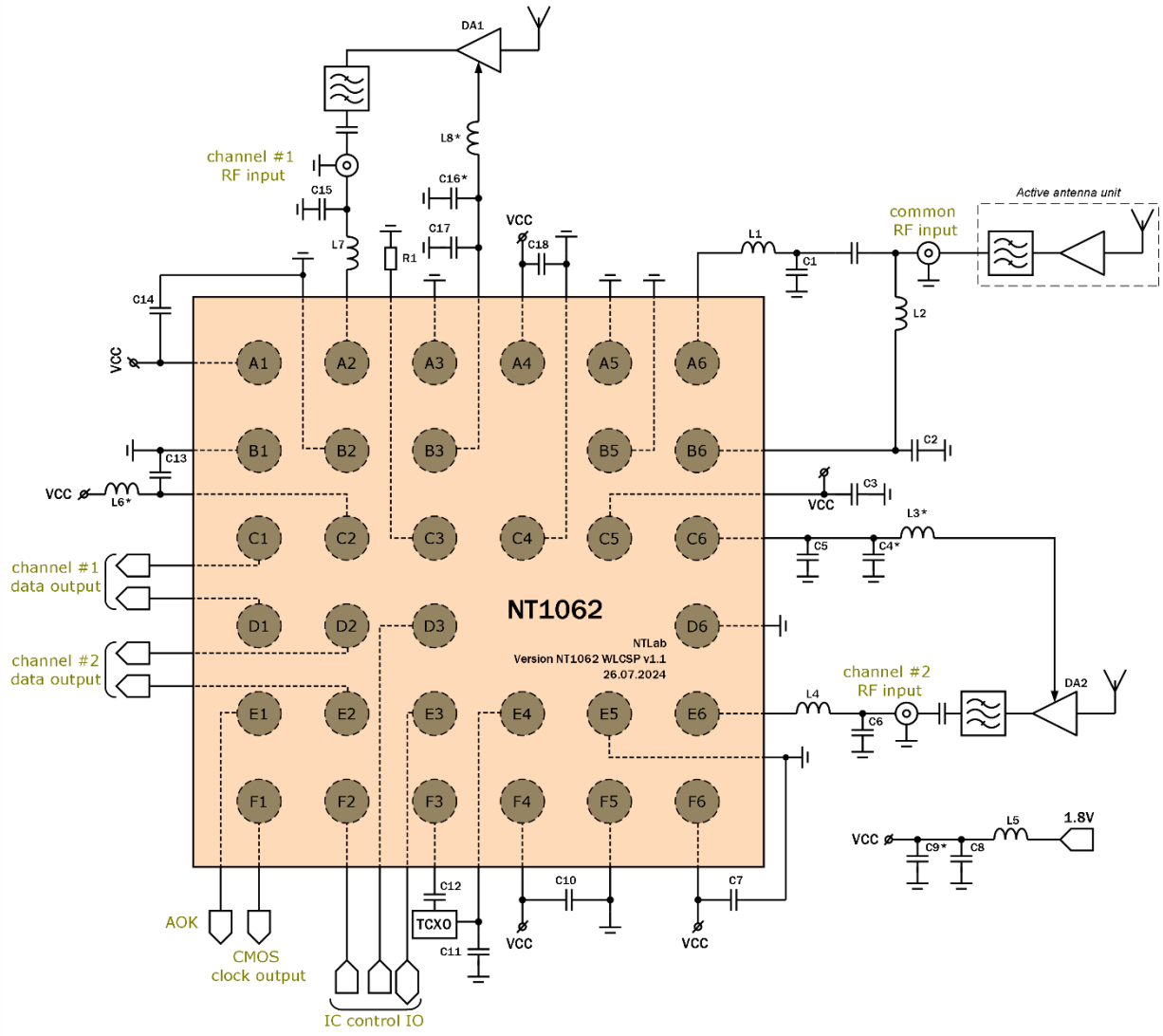


Figure 4.6: NT1062 WLCSP (top view) application schematic

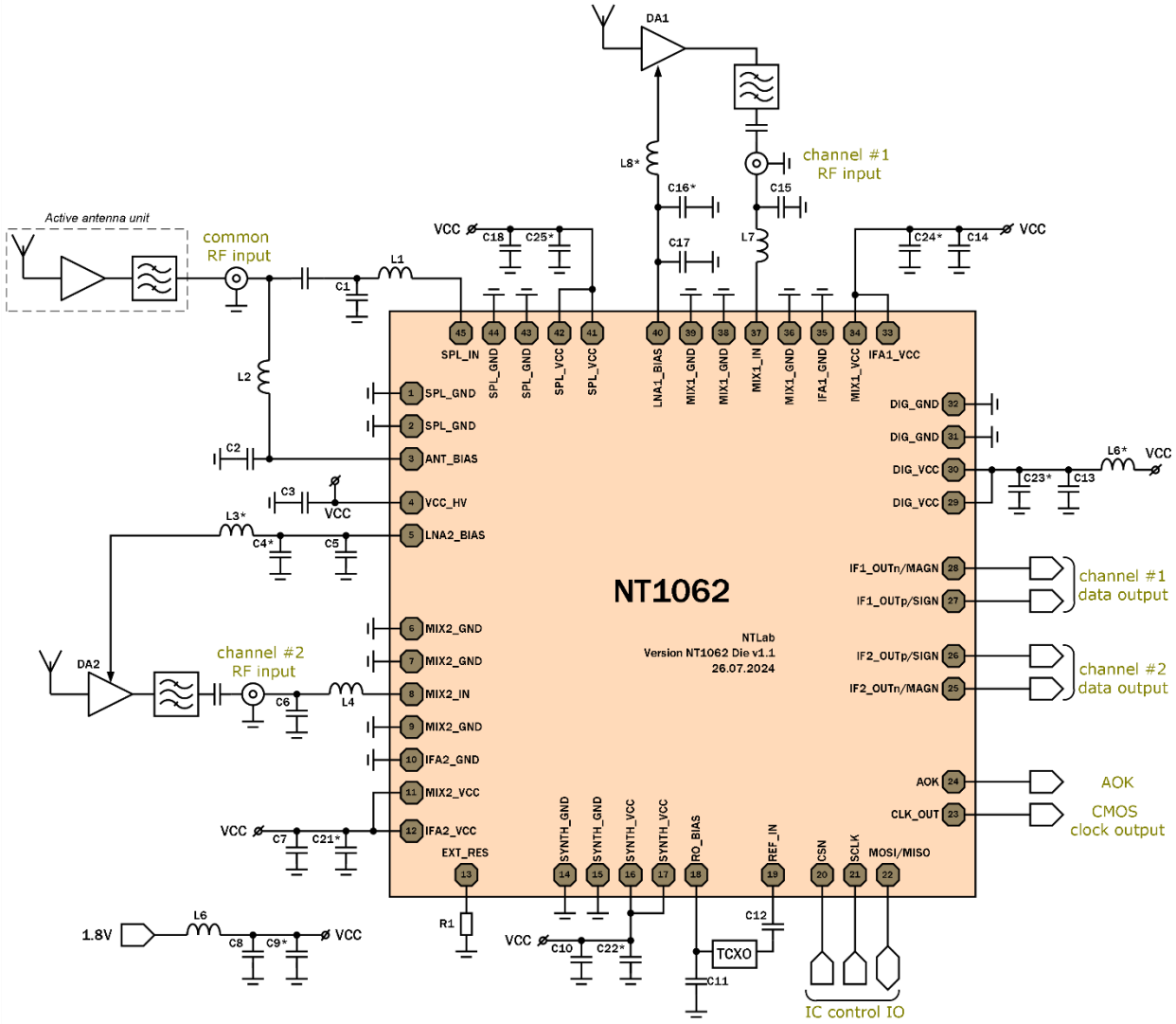


Figure 4.7: NT1062 bare die application schematic

Table 4.1: External components description

Component	Nominal value	Tolerance	Notes
C1	1.5pF	±5%	Matching network capacitor
C2	10nF	±10%	Supply voltage filtering capacitor
C3	0.33µF	±10%	Supply voltage filtering capacitor
C4*	2.2µF	±10%	Supply voltage filtering capacitor
C5	33nF	±10%	Supply voltage filtering capacitor
C6	3.9pF	±5%	Matching network capacitor for L5 band
	3.0pF	±5%	Matching network capacitor for L3 band
	5.6pF	±5%	Matching network capacitor for L2 band
	6.0pF	±5%	Matching network capacitor for E6 band
C7	0.1µF	±10%	Supply voltage filtering capacitor
C8	10µF	±10%	Supply voltage filtering capacitor
C9*	2.2µF	±10%	Supply voltage filtering capacitor
C10	0.1µF	±10%	Supply voltage filtering capacitor
C11	0.1µF	±10%	Supply voltage filtering capacitor

Component	Nominal value	Tolerance	Notes
C12	100pF	±10%	Blocking capacitor**
C13	0.1µF	±10%	Supply voltage filtering capacitor
C14	0.1µF	±10%	Supply voltage filtering capacitor
C15	3.3pF	±5%	Matching network capacitor for L1 band
C16*	2.2µF	±10%	Supply voltage filtering capacitor
C17	33nF	±10%	Supply voltage filtering capacitor
C18	0.1µF	±10%	Supply voltage filtering capacitor
C19	10µF	±10%	Supply voltage filtering capacitor
C20	2.2µF	±10%	Supply voltage filtering capacitor
C21*	0.1µF	±10%	Supply voltage filtering capacitor
C22*	0.1µF	±10%	Supply voltage filtering capacitor
C23*	0.1µF	±10%	Supply voltage filtering capacitor
C24*	0.1µF	±10%	Supply voltage filtering capacitor
C25*	0.1µF	±10%	Supply voltage filtering capacitor
L1	8.2nH	±2%	Matching network inductor
L2	56nH	±5%	AC blocking inductor
L3*	470Ohm/ 100MHz	±20%	Supply voltage filtering inductor
L4	15nH	±2%	Matching network inductor for L5 band
	15nH	±2%	Matching network inductor for L3 band
	13nH	±2%	Matching network inductor for L2 band
	12nH	±2%	Matching network inductor for E6 band
L5	470Ohm/ 100MHz	±20%	Supply voltage filtering inductor
L6*	470Ohm/ 100MHz	±20%	Supply voltage filtering inductor
L7	9.1nH	±2%	Matching network inductor for L1 band
L8*	470Ohm/ 100MHz	±20%	Supply voltage filtering inductor
L9	470Ohm/ 100MHz	±20%	Supply voltage filtering inductor
R1	61.9kOhm	±1%	High precision resistor
DA1	MAX2659	–	Recommended external amplifier for L1 band
DA2	MAX2691	–	Recommended external amplifier for L2, L3, L5 bands

* Not obligatory to use
** Depends on TCXO output signal level

4.3. PINS DESCRIPTION

Table 4.2: NT1062 pins and pads description

Pin	Pad	Ball	Name	Description
1	1 2	A5 B5 C4	SPL_GND	Splitter ground
2	3	B6	ANT_BIAS	External active antenna supply voltage
3	4	C5	VCC_HV	Active antenna detector supply voltage (3.3V or 1.8V)
4	5	C6	LNA2_BIAS	External LNA#2 supply voltage (1.8V)
5	6 7	D6 E5	MIX2_GND	Mixer#2 ground
6	8	E6	MIX2_IN	Mixer#2 input
7	9	D6	MIX2_GND	Mixer#2 ground
	10	E5	IFA2_GND	IFA#2 ground
8	11	F6	MIX2_VCC	Mixer#2 supply voltage (1.8V)
	12		IFA2_VCC	IFA#2 supply voltage (1.8V)
9	13	C3	EXT_RES	External resistor for reference current source
10	14	F5	SYNTH2_GND	PLL#2 ground
	15		SYNTH1_GND	PLL#1 ground
11	16	F4	SYNTH1_VCC	PLL#1 supply voltage (1.8V)
	17		SYNTH2_VCC	PLL#2 supply voltage (1.8V)
12	18	E4	RO_BIAS	External reference oscillator supply voltage (1.8V)
13	19	F3	REF_IN	Reference frequency input
14	20	D3	CSN	SPI chip select
15	21	F2	SCLK	SPI clock input
16	22	E3	MOSI/ MISO	SPI data input/output
17	23	F1	CLK_OUT	Clock frequency CMOS output
18	24	E1	AOK	Cumulative status indicator: “1” valid “0” fail
19	25	E2	IF2_OUTn/MAGN	Channel#2 analog output – complement; 2-bit ADC digital output data – MAGN
20	26	D2	IF2_OUTp/SIGN	Channel#2 analog output – true; 2-bit ADC digital output data – SIGN
21	27	D1	IF1_OUTp/SIGN	Channel#1 analog output – true; 2-bit ADC digital output data – SIGN
22	28	C1	IF1_OUTn/MAGN	Channel#1 analog output – complement; 2-bit ADC digital output data – MAGN
23	29 30	C2	DIG_VCC	ADCs supply voltage (1.8V)
24	31 32	B1	DIG_GND	ADCs ground
25	33	A1	IFA1_VCC	IFA#1 supply voltage (1.8V)
	34		MIX1_VCC	Mixer#1 supply voltage (1.8V)
26	35	A3	IFA1_GND	IFA#2 ground
	36	B2	MIX1_GND	Mixer#1 ground
27	37	A2	MIX1_IN	Mixer#1 input

Pin	Pad	Ball	Name	Description
28	38	A3	MIX1_GND	Mixer#1 ground
	39	B2		
29	40	B3	LNA1_BIAS	External LNA#1 supply voltage (1.8V)
30	41	A4	SPL_VCC	Splitter supply voltage (1.8V)
	42			
31	43	A5	SPL_GND	Splitter ground
	44	B5		
		C4		
32	45	A6	SPL_IN	Splitter input

Table 4.3: NT1062 balls description

Ball	Pad	Pin	Name	Description
A1	33	25	IFA1_VCC	IFA#1 supply voltage (1.8V)
	34		MIX1_VCC	Mixer#1 supply voltage (1.8V)
A2	37	27	MIX1_IN	Mixer#1 input
A3	35	26	IFA1_GND	IFA#2 ground
	36		MIX1_GND	Mixer#1 ground
	38	28	MIX1_GND	Mixer#1 ground
	39		MIX1_GND	Mixer#1 ground
A4	41	30	SPL_VCC	Splitter supply voltage (1.8V)
	42		SPL_VCC	Splitter supply voltage (1.8V)
A5	43	31	SPL_GND	Splitter ground
	44		SPL_GND	Splitter ground
	1	1	SPL_GND	Splitter ground
	2		SPL_GND	Splitter ground
A6	45	32	SPL_IN	Splitter input
B1	31	24	DIG_GND	ADCs ground
	32		DIG_GND	ADCs ground
B2	35	26	IFA1_GND	IFA#2 ground
	36		MIX1_GND	Mixer#1 ground
	38	28	MIX1_GND	Mixer#1 ground
	39		MIX1_GND	Mixer#1 ground
B3	40	29	LNA1_BIAS	External LNA#1 supply voltage (1.8V)
B5	43	31	SPL_GND	Splitter ground
	44		SPL_GND	Splitter ground
	1	1	SPL_GND	Splitter ground
	2		SPL_GND	Splitter ground
B6	3	2	ANT_BIAS	External active antenna supply voltage
C1	28	22	IF1_OUTn/MAGN	Channel#1 analog output – complement; 2-bit ADC digital output data – MAGN
C2	29	23	DIG_VCC	ADCs supply voltage (1.8V)
	30			
C3	13	9	EXT_RES	External resistor for reference current source
C4	43	31	SPL_GND	Splitter ground
	44		SPL_GND	Splitter ground
	1	1	SPL_GND	Splitter ground
	2		SPL_GND	Splitter ground

Ball	Pad	Pin	Name	Description
C5	4	3	VCC_HV	Active antenna detector supply voltage (3.3V or 1.8V)
C6	5	4	LNA2_BIAS	External LNA#2 supply voltage (1.8V)
D1	27	21	IF1_OUTp/SIGN	Channel#1 analog output – true; 2-bit ADC digital output data – SIGN
D2	26	20	IF2_OUTp/SIGN	Channel#2 analog output – true; 2-bit ADC digital output data – SIGN
D3	20	14	CSN	SPI chip select
D6	6	5	MIX2_GND	Mixer#2 ground
	7		MIX2_GND	Mixer#2 ground
	9	7	MIX2_GND	Mixer#2 ground
	10		IFA2_GND	IFA#2 ground
E1	24	18	AOK	Cumulative status indicator: “1” valid “0” fail
E2	25	19	IF2_OUTn/MAGN	Channel#2 analog output – complement; 2-bit ADC digital output data – MAGN
E3	22	16	MOSI/ MISO	SPI data input/output
E4	18	12	RO_BIAS	External reference oscillator supply voltage (1.8V)
E5	6	5	MIX2_GND	Mixer#2 ground
	7		MIX2_GND	Mixer#2 ground
	9	7	MIX2_GND	Mixer#2 ground
	10		IFA2_GND	IFA#2 ground
E6	8	6	MIX2_IN	Mixer#2 input
F1	23	17	CLK_OUT	Clock frequency CMOS output
F2	21	15	SCLK	SPI clock input
F3	19	13	REF_IN	Reference frequency input
F4	16	11	SYNTH1_VCC	PLL#1 supply voltage (1.8V)
	17		SYNTH2_VCC	PLL#2 supply voltage (1.8V)
F5	14	10	SYNTH2_GND	PLL#2 ground
	15		SYNTH1_GND	PLL#1 ground
F6	11	8	MIX2_VCC	Mixer#2 supply voltage (1.8V)
	12		IFA2_VCC	IFA#2 supply voltage (1.8V)

4.4. SERIAL INTERFACE DESCRIPTION

4.4.1. PROTOCOL DESCRIPTION

NT1062 can be configured with standard 3-wire SPI. In addition special pin “AOK” (low level interrupt) for unexpected system failure tracking is available.
Serial interface is used to read and change NT1062 data register information. It is intended for status monitoring, mode configuration and parameter adjustment.

4.4.1.1. GENERAL DESCRIPTION

Serial interface uses 3 pins for communication:

- CSN (serial interface chip select signal with low active level)
- SCLK (serial interface clock)
- MOSI/MISO (serial interface input/output data)

Serial interface structure is shown on Figure 4.8.

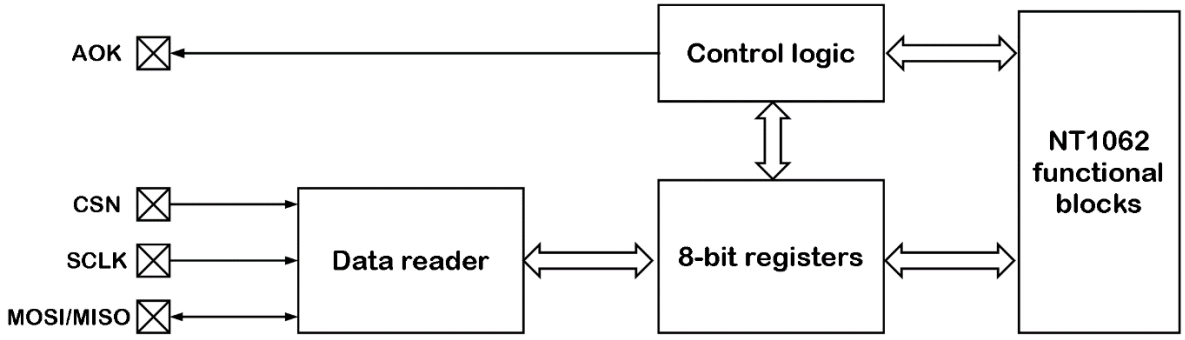


Figure 4.8: Serial interface structure

Data reader is intended for data exchange between 8-bit registers and external control unit using 3-wire serial bus. Data reader takes or changes values of internal trigger cells in the block of 8-bit registers. Internal trigger cells control internal blocks of NT1062 directly or through some logic elements.
Standard information packet (command) consists of two bytes and includes read/write attribute, 7-bit address and 8-bit data. The first bit of a command is a read/write attribute: read operation is defined by “1” and write operation is defined by “0”. A6…A0 bits represent address of the register to be read or written. D7…D0 bits are data to be read or written to the given address.
Communication is initialized by setting CSN to “0”. SCLK must be low at the beginning of any data transfer (falling CSN edge). Data format is always a bit sequence from first MSB to last LSB. All data transfers are framed by CSN signal, which must be low for any data transfer. In “idle” state, when CSN is high, SCLK and MOSI/MISO pins are blocked and don’t respond to external signals.

4.4.1.2. INFORMATION WRITING TO THE REGISTER

Single register writing is shown on Figure 4.9. Read/write attribute is set to “0” for writing mode. Data is sampled into the NT1062 through the MOSI/MISO pin on the rising edges of SCLK. After CSN is set to “0”, first 8 bits of the command (write attribute and register address) will be written to the interface on the 8 rising edges of SCLK. On the next 8 rising edges of SCLK D<7:0> data will be received. After that any rising edge of SCLK will be ignored. D<7:0> data will be written to the known address A<6:0> after last falling edge of SCLK.

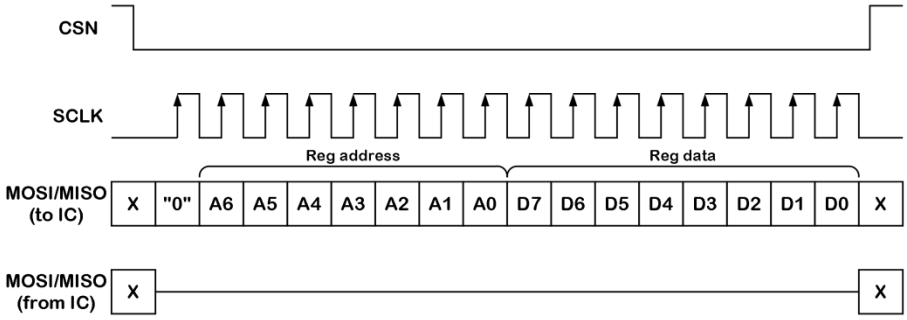


Figure 4.9: Individual register writing

4.4.1.3. INFORMATION READING FROM THE REGISTER

Single register reading is shown on Figure 4.10. Read/write attribute is set to "1" for reading mode. Data is sampled out of the NT1062 through the MOSI/MISO pin on the falling edges of SCLK. After CSN is set to "0", first 8 bits of the command (read attribute and register address) will be written to the interface on the 8 rising edges of SCLK. On the next 8 falling edges of SCLK D<7:0> data from the register with A<6:0> address will be send to MOSI/MISO pin. D<7:0> data can be sampled by external control unit on the rising edge of SCLK. After data byte receiving CSN goes high, disabling the interface.

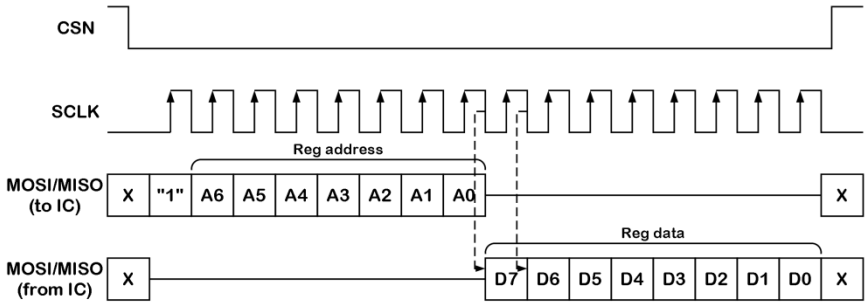


Figure 4.10: Individual register reading

4.4.1.4. BURST DATA TRANSFER

NT1062 has a SPI burst-mode data transfer. Unlike single data transfer CSN should be still "0" after LSB of the first data byte. CSN goes high to stop burst data transfer after the LSB of the last data byte.

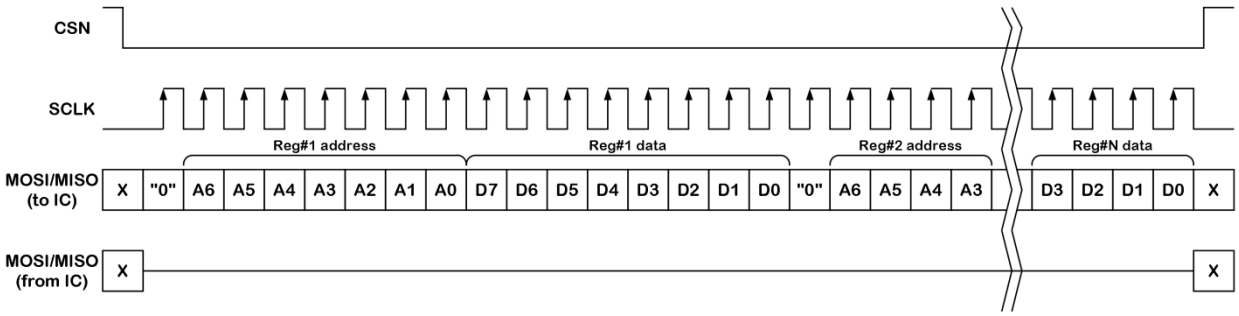


Figure 4.11: Burst register writing

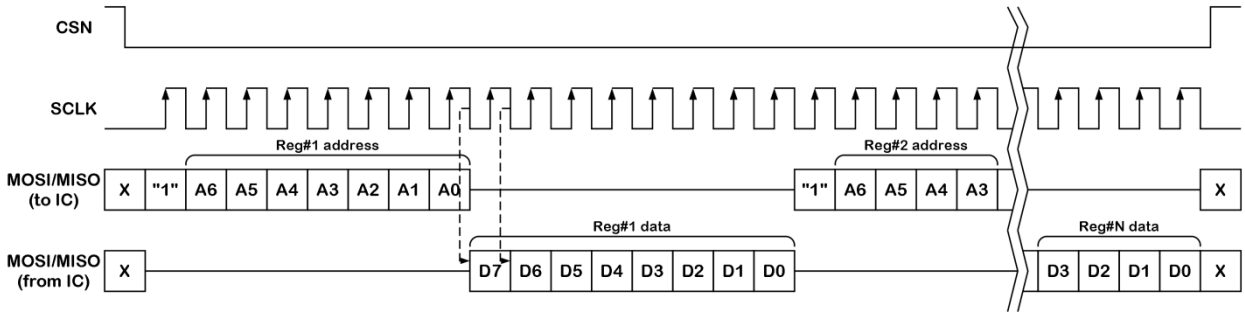


Figure 4.12: Burst register reading

4.4.1.5. TIMING DIAGRAM

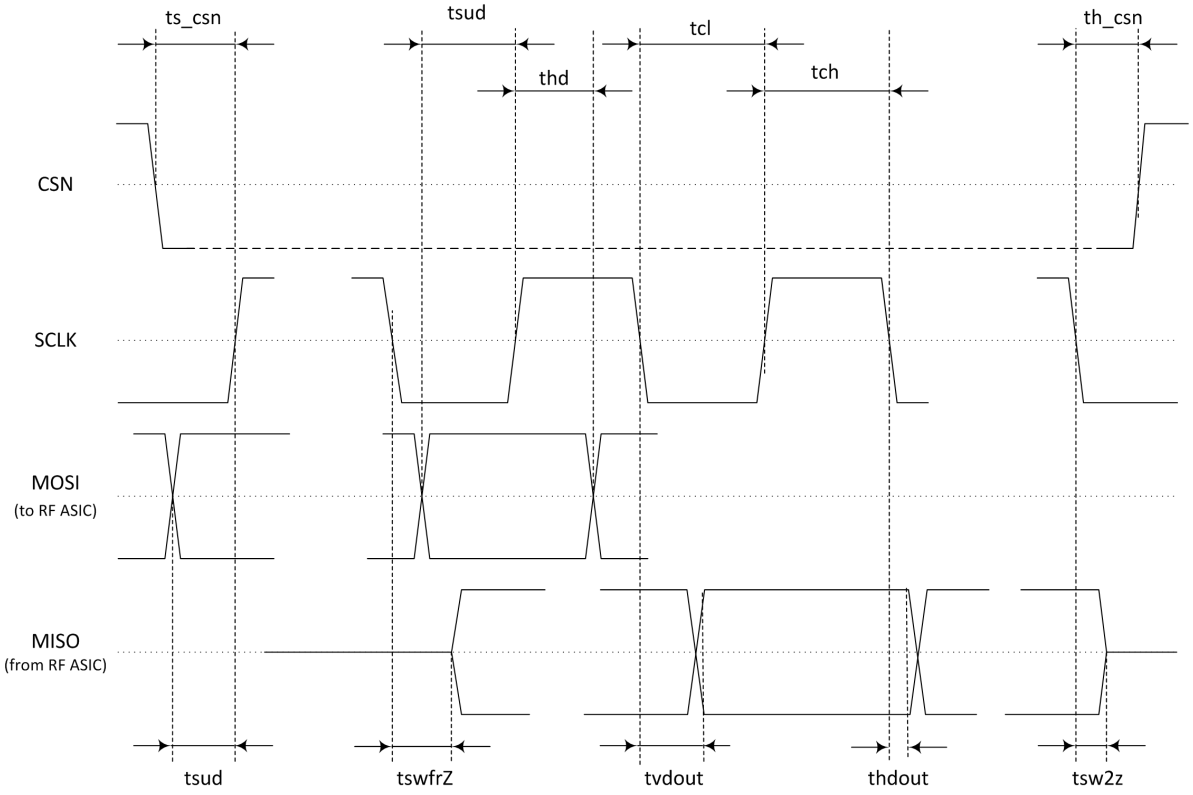


Figure 4.13: SPI timing diagram

Table 4.4: SPI timing

Parameter description	Symbol	Condition	Value			Unit
			min	typ.	max	
SCLK frequency	fclk	–	–	–	40	MHz
SCLK high and low time	tch tcl	1/fclk = (tch+tcl)	8	–	12	ns
Duty cycle	D	–	40	–	60	%
CSN setup time before SCLK	ts_csn	–	8	–	–	ns
CSN hold time	th_csn	–	4	–	–	ns
Data set up time	tsud	–	10	–	–	ns
Data hold time	thd	–	3	–	–	ns
Switch from Z-state time	tswfrZ	Load 20 pF	–	–	10	ns
Output data hold time	thdout	Load 20 pF	2.8	–	–	ns
Output data valid time	tvdout	Load 20 pF	–	–	10	ns
Switch to Z-state time	tsw2z	Load 20 pF	3	–	8	ns

4.4.2. PROGRAMMABLE REGISTERS

System information:

- Chip serial number, chip version, GDS version

General settings and status:

- General status (common AOK, reference frequency indicator, die temperature, battery level indicator)
- Common AOK indicator configuration (6 bits)
- Common AOK output enable
- Battery level indicator enable
- Battery level indicator threshold (3 bits)
- IC mode (active modes, standby)
- Reference frequency //valid range is 10-40MHz
- External reference oscillator (TCXO) supply circuit enable
- General purpose outputs enable (2 bits)
- General purpose outputs level (low, high)
- Temperature measurement mode (single, continuous)
- Temperature measurement execution
- Temperature measurement status (valid, fail)

Channels #1 and #2 settings and status:

- Channel sideband (upper, lower)
- IF passband (7 bits)
- Output data interface (2-bit ADC, analog differential)
- IF GC mode (automatic, manual via SPI)
- IF gain (10 bits) //if manual GC mode
- IFA AGC digital detector thresholds //if 2-bit ADC output and automatic IF GC mode
- IFA output amplitude (2 bits) //if analog output and automatic IF GC mode
- 2-bit ADC type (synchronous, asynchronous) //if 2-bit ADC output

Active antenna detection system settings and status:

- Active antenna detector enable
- Active antenna supply voltage output (1.8V, 2.4V, 2.7V, 3.0V)
- Active antenna current (3 bits)
- Active antenna detector input level indicator
- Active antenna connection indicator

Synthesizers #1 and #2 settings and status:

- R-divider ratio (:1, :2)
- N-divider ratio (10 bits)
- Fractional-N mode enable
- F-divider ratio (24 bits) //if fractional-N mode
- Tuning system execute
- Status (lock indicator, VCO voltage comparator status)

CLK settings:

- Clock output buffer enable
- Clock frequency and ADC sampling frequency source (PLL#1, PLL#2, pass-through)
- C-divider ratio (10 bits) //if clock frequency source is PLL#1 or PLL#2
- Clock output signal front (2 bits)

Bit number	Description		Default
Reg0, 0x00			
D7–D0	chip_id<12:5>	Chip serial number. $(0010000100110)_{dec}$ = 1062	"00100001"
Reg1, 0x01			
D7–D3	chip_id<4:0>	Continue. Refer to Reg0<D7–D0>.	"00110"
D2–D0	chip_rev<2:0>	Chip version. $(001)_{dec}$ = 1	"001"
Reg2, 0x02			
D7	PLL3G_RDIV_ON	Channel #1 PLL R-divider ratio: "0" 1 "1" 2	"0"
D6	PLL2G_RDIV_ON	Channel #2 PLL R-divider ratio: "0" 1 "1" 2	"0"
D5	CLK_RO_ON	TCXO pass-through mode: "0" disabled "1" enabled **Note:** Available if PLL3G_CDIV_EN = "0" and PLL2G_CDIV_EN = "0".	"1"
D4	CLK_IFA1_ON	Channel #1 ADC synchronous mode (if IFA1_enADC = "1"): "0" disabled "1" enabled	"1"
D3	CLK_IFA2_ON	Channel #2 ADC synchronous mode (if IFA2_enADC = "1"): "0" disabled "1" enabled	"1"
D2–D0	IC_MODE<2:0>	IC mode: "x00" standby "001" Ch#1 RF input (pin #27) "010" Ch#2 RF input (pin #6) "011" Ch#1 + Ch#2 RF inputs (pins #27 and #6) "101" Ch#1 splitter input (pin #32) "110" Ch#2 splitter input (pin #32) "111" Ch#1 + Ch#2 splitter input (pin #32)	"000"
Reg3, 0x03			
D7-D6	Unused	Unused	"00"
D5–D0	XTAL_CLK_DIV<5:0>	Reference frequency setting (valid range is 10-40MHz): "000000" unused … … "001001" unused "001010" 9.501 … 10.500 MHz "001011" 10.501 … 11.500 MHz … with step of 1 MHz "010000" 15.501 … 16.500 MHz … with step of 1 MHz "101000" 39.501 … 40.5 MHz "101001" unused … … "111111" unused	"010000"
Reg4, 0x04			
D7–D6	Unused	Unused	"00"
D5	GPO1	General purpose output: "0" logic "0" "1" logic "1" **Note:** Available at pin #17 if CLK_OUT<1:0> = "11" and TEST_GPO1_EN = "1".	"0"

Bit number	Description		Default
D4	GPO0	General purpose output: “0” logic “0” “1” logic “1” **Note:** Available at pin #18 if CLK_OUT <1:0> = “10” or “11” and TEST_GPO0_EN = “1”.	“0”
D3–D2	Service settings	Do not change	“00”
D1–D0	CLK_OUT<1:0>	Clock output mode: “00” pin#17 CMOS pin#18 AOK “01” n/a n/a “10” CMOS GPO0 “11” GPO1 GPO0	“00”
Reg5, 0x05			
D7	aok_mask_PLL3G_SAS	Channel #1 SAS voltage comparators status as common AOK’s component: “0” forbidden “1” permitted	“1”
D6	aok_mask_PLL3G_LD	Channel #1 PLL lock detector status as common AOK’s component: “0” forbidden “1” permitted	“1”
D5	aok_mask_PLL2G_SAS	Channel #2 SAS voltage comparators status as common AOK’s component: “0” forbidden “1” permitted	“1”
D4	aok_mask_PLL2G_LD	Channel #2 PLL lock detector status as common AOK’s component: “0” forbidden “1” permitted	“1”
D3	Service setting	Do not change	“0”
D2	aok_mask_MFD	Reference frequency detector status as common AOK’s component: “0” forbidden “1” permitted	“1”
D1	Service setting	Do not change	“0”
D0	aok_mask_LBI	Battery level indicator as common AOK’s component: “0” forbidden “1” permitted	“1”
Reg6, 0x06			
D7	CLK_BUF_EN	Clock frequency output buffer: “0” disabled “1” enabled **Note:** Automatically enabled when one of active modes is selected (when IC_MODE<2:0> ≠ “X00”).	“0”
D6	Service setting	Do not change	-
D5	RO_BIAS_EN	Reference oscillator (TCXO) supply circuit: “0” disabled “1” enabled **Note:** Automatically enabled when one of active modes is selected (when IC_MODE<2:0>≠“X00”)	“0”
D4–D0	Service settings	Do not change	-

Bit number	Description		Default
Reg7, 0x07			
D7	LBI_EN	Battery level indicator: "0" disabled "1" enabled	"0"
		Note: Automatically enabled when one of active modes is selected (when IC_MODE<2:0>≠"X00").	
D6	Service setting	Do not change	-
D5	ANT_EN	Active antenna detector: "0" disabled "1" enabled	"0"
		Note: Automatically enabled when one of active modes is selected (when IC_MODE<2:0>≠"X00").	
D4–D0	Service settings	Do not change	-
Reg8, 0x08			
D7–D6	Unused	Unused	"00"
D5–D2	Service settings	Do not change	-
D1	PLL3G_DSM_EN	Channel #1 delta-sigma modulator (for operating in fractional-N mode of PLL #1): "0" disabled "1" enabled	"0"
D0	PLL3G_CDIV_EN	Channel #1 C-divider: "0" disabled "1" enabled	"0"
		Note: Available if PLL2G_CDIV_EN = "0" and CLK_RO_ON = "0".	
Reg9, 0x09			
D7–D6	Unused	Unused	"00"
D5–D2	Service settings	Do not change	-
D1	PLL2G_DSM_EN	Channel #2 delta-sigma modulator (for operating in fractional-N mode of PLL #2): "0" disabled "1" enabled	"0"
D0	PLL2G_CDIV_EN	Channel #2 C-divider: "0" disabled "1" enabled	"0"
		Note: Available if PLL3G_CDIV_EN = "0" and CLK_RO_ON = "0".	
Reg10, 0x0A			
D7–D2	Unused	Unused	"000000"
D1	Service setting	Do not change	"1"
D0	TMStart	Temperature measurement execution: "0" finished "1" start (automatically reset to "0" when finished)	"0"

Bit number	Description		Default
Reg11, 0x0B			
D7–D3	Unused	Unused	“00000”
D2	TS_ready	Temperature sensor status: “0” measurement in progress “1” measurement finished	-
D1–D0	Tcode<9:8>	Temperature sensor indicator: $T = -266.21 + 0.654 \times (Tcode < 9:0 >_{dec})$ “0000000000” not valid range … … “1000101111” not valid range “1000110000” +100°C “0110111101” +25°C “0101011010” -40°C “0101011011” not valid range … … “1111111111” not valid range	-
Reg12, 0x0C			
D7–D0	Tcode<7:0>	Continue. Refer to Reg11<D1–D0>.	-
Reg13, 0x0D			
D7–D5	Service settings	Do not change	“101”
D4–D2	ANT_VCur<2:0>	Active antenna current: “000” n/a “001” 3 mA “010” 5 mA “011” 7 mA “100” 9 mA “101” 11 mA “110” 13 mA “111” 15 mA	“100”
D1–D0	ANT_Vout<1:0>	Active antenna supply voltage output: VCC_HV = 3.3V / VCC_HV = 1.8V “00” 1.8V / 1.8V “01” 2.4V / n/a “10” 2.7V / n/a “11” 3.0V / n/a	“00”
Reg14, 0x0E			
D7	Unused	Unused	“0”
D6	AOK	Common cumulative status indicator: “0” fail “1” valid **Note:** Available at pin #18 if CLK_OUT<1:0> = “00” and TEST_GPO0_EN = “1”.	-
D5	Service setting	May change its state	-
D4	MFD_OUT	Reference frequency indicator: “0” ≥150kHz “1” <150kHz	-
D3	LBI	Battery level indicator status: “0” Battery level > LBI_Lvl<2:0> “1” Battery level < LBI_Lvl<2:0>	-
D2	ANT_LV	Active antenna detector input level indicator: “0” valid “1” low voltage (VCC_HV is too low)	-

Bit number	Description		Default
D1	Service setting	May change its state	-
D0	ANT_Used	Active antenna connection indicator: "0" not connected (active antenna current is too low) "1" connected (active antenna current is within limits)	-
Reg15, 0x0F			
D7–D6	Unused	Unused	"00"
D5–D0	Service settings	Do not change	"010101"
Reg16, 0x10			
D7–D6	Unused	Unused	"00"
D5–D0	Service settings	Do not change	"001111"
Reg17, 0x11			
D7	Unused	Unused	"0"
D6	MIX1_USB	Channel #1 sideband: "0" lower "1" upper	"1"
D5–D0	Service settings	Do not change	"010000"
Reg18, 0x12			
D7–D5	Unused	Unused	"000"
D4–D0	Service settings	Do not change	"00101"
Reg19, 0x13			
D7	Unused	Unused	"0"
D6	MIX2_USB	Channel #2 sideband: "0" lower "1" upper	"1"
D5–D0	Service settings	Do not change	"010000"
Reg20, 0x14			
D7–D5	Unused	Unused	"000"
D4–D0	Service settings	Do not change	"00101"
Reg21, 0x15			
D7–D4	Unused	Unused	"0000"
D3	IFA1_enADC	Channel #1 output data interface type: "0" analog differential "1" 2-bit ADC	"1"
D2	IFA1_digDet_En	Channel #1 IFA digital detector: "0" disabled "1" enabled **Note:** Must be disabled if IFA1_enADC = "0".	"1"
D1	Service setting	Do not change	"1"
D0	IFA1_agc_En	Channel #1 IFA gain control mode: "0" manual "1" automatic	"1"

Bit number	Description			Default
Reg22, 0x16				
D7–D2	Service settings	Do not change		“100110”
D1–D0	IFA1_dac<9:8>	Channel #1 IFA gain value (if IFA1_agc_En = “0”): “0000000000” 68.0 dB … “0010110100” 68.0 dB … “0101011110” 57.9 dB … “0111010110” 49.1 dB … “1000100110” 37.3 dB … “1010010100” 27.2 dB … “1011101110” 17.5 dB … “1100010110” 10.5 dB … “1101011100” 0.27 dB	Channel #1 IFA digital detector threshold w.r.t. sinewave signal (if IFA1_agc_En = “1” and IFA1_enADC = “1”): “0000000000” not available … “0100101100” 69.5% … “0110010000” 60.0% … “0111110100” 50.4% … “1001011000” 40.6% … “1011001100” 29.2% … “1110000100” 10.8% … “1111111111” not available	“10”
Reg23, 0x17				
D7–D0	IFA1_dac<7:0>	Continue. Refer to Reg22<D1–D0>.		“11001100”
Reg24, 0x18				
D7	Unused	Unused		“0”
D6–D2	Service settings	Do not change		“10010”
D1–D0	IFA1_det_ALC<1:0>	Channel #1 IFA output amplitude: “00” 78mV “01” 90mV “10” 100mV “11” 116mV **Note:** Available if IFA1_agc_En = “1” and IFA1_enADC = “0”.		“10”
Reg25, 0x19				
D7	Unused	Unused		“0”
D6–D0	LPF1_ctr_def<6:0>	Channel #1 LPF cut-off frequency: “0000000” not used … “0001011” not used “0001100” 4.2 MHz “0011000” 5.2 MHz – default value “0011111” 6.5 MHz “0100011” 7.2 MHz “0100111” 8.1 MHz “0101011” 9.0 MHz “0110000” 10.2 MHz “0110101” 11.7 MHz “0111010” 13.1 MHz “0111111” 14.6 MHz “1000100” 16.2 MHz “1001000” 17.5 MHz “1001100” 18.8 MHz “1001101” not used … “1111111” not used		“0011000”

Bit number	Description		Default
Reg26, 0x1A			
D7–D4	Unused		"0000"
D3	IFA2_enADC	Channel #2 output data interface type: "0" analog differential "1" 2-bit ADC	"1"
D2	IFA2_digDet_En	Channel #2 IFA digital detector: "0" disabled "1" enabled **Note:** Must be disabled if IFA2_enADC = "0".	"1"
D1	Service setting	Do not change	"1"
D0	IFA2_agc_En	Channel #2 IFA gain control mode: "0" manual "1" automatic	"1"
Reg27, 0x1B			
D7–D2	Service settings	Do not change	"101110"
D1–D0	IFA2_dac<9:8>	Channel #2 IFA gain value (if IFA2_agc_En = "0"): "0000000000" 68.0 dB … "0010110100" 68.0 dB … "0101011110" 57.9 dB … "0111010110" 49.1 dB … "1000100110" 37.3 dB … "1010010100" 27.2 dB … "1011101110" 17.5 dB … "1100010110" 10.5 dB … "1101011100" 0.27 dB Channel #2 IFA digital detector threshold w.r.t. sinewave signal (if IFA2_agc_En = "1" and IFA2_enADC = "1"): "0000000000" not available … "0100101100" 69.5% … "0110010000" 60.0% … "0111110100" 50.4% … "1001011000" 40.6% … "1011001100" 29.2% … "1110000100" 10.8% … "1111111111" not available	"10"
Reg28, 0x1C			
D7–D0	IFA2_dac<7:0>	Continue. Refer to Reg27<D1–D0>.	"11001100"
Reg29, 0x1D			
D7	Unused	Unused	"0"
D6–D2	Service settings	Do not change	"10010"
D1–D0	IFA2_det_ALC<1:0>	Channel #2 IFA output amplitude control: "00" 78mV "01" 90mV "10" 100mV "11" 116mV **Note:** Available if IFA2_agc_En = "1" and IFA2_enADC = "0"	"10"

Bit number	Description		Default
Reg30, 0x1E			
D7	Service setting	Do not change	"0"
D6–D0	LPF2_ctr_def<6:0>	Channel #2 LPF cut-off frequency: "0000000" not used … … "0001011" not used "0001100" 4.2 MHz "0011000" 5.2 MHz "0011111" 6.5 MHz "0100011" 7.2 MHz – default value "0100111" 8.2 MHz "0101011" 9.2 MHz "0110000" 10.5 MHz "0110101" 12.1 MHz "0111010" 13.6 MHz "0111111" 15.2 MHz "1000100" 17.0 MHz "1001000" 18.5 MHz "1001100" 19.9 MHz "1001101" not used … … "1111111" not used	"0100011"
Reg31, 0x1F			
D7–D0	Service settings	Do not change	"00000000"
Reg32, 0x20			
D7–D6	Unused	Unused	"00"
D5–D2	Service settings	Do not change	"0110"
D1–D0	PLL3G_CDiv<9:8>	Channel #1 C-divider ratio (refer to formula in section 7.10 for F_{CLK} calculation): "0000000000" unused … unused "0000010100" unused "0000010101" 21 … with step of 1 "1111111111" 1023 **Note:** Available if PLL3G_CDIV_EN = "1".	"00"
Reg33, 0x21			
D7–D0	PLL3G_CDiv<7:0>	Continue. Refer to Reg32 <D1-D0>.	"01010000"
Reg34, 0x22			
D7–D0	Service settings	Refer to section 7.6.	"00001100"
Reg35, 0x23			
D7–D2	Unused	Unused	"000000"
D1–D0	PLL3G_NDiv<9:8>	Channel #1 N-divider ratio (refer to formula in section 7.5 for F_{LO} calculation): "0000000000" unused … unused "0000101001" unused "0000101010" 42 … with step of 1 "1111111111" 1023	"00"
Reg36, 0x24			
D7–D0	PLL3G_NDiv<7:0>	Continue. Refer to Reg35 <D1-D0>.	"11000000"

Bit number	Description		Default
Reg37, 0x25			
D7–D0	PLL3G_DSM_N<23:16>	Channel #1 N-divider fractional ratio (F-divider). Refer to formula in section 7.5 for F_{LO} calculation. 0_{dec} N-divider ratio is integer other N-divider ratio is fractional PLL3G_DSM_N<23:0>=fraction*2^{24}	"00000000"
Reg38, 0x26			
D7–D0	PLL3G_DSM_N<15:8>	Continue. Refer to Reg38 <D7–D0>.	"00000000"
Reg39, 0x27			
D7–D0	PLL3G_DSM_N<7:0>	Continue. Refer to Reg38 <D7–D0>.	"00000000"
Reg40, 0x28			
D7–D6	Unused	Unused	"00"
D5–D0	Service settings	Refer to section 7.6.	"010110"
Reg41, 0x29			
D7–D0	Service settings	Refer to section 7.6.	"10001001"
Reg42, 0x2A			
D7–D5	Unused	Unused	"000"
D4–D0	Service settings	Refer to section 7.6.	"00000"
Reg43, 0x2B			
D7–D4	Unused	Unused	"0000"
D3	Service setting	May change its state	-
D2–D1	PLL3G_SAS_CMPH PLL3G_SAS_CMPL	Channel #1 VCO voltage comparator status: "00" valid "01" lower threshold exceeded (oscillation frequency is too low) "10" upper threshold exceeded (oscillation frequency is too high) "11" unused	-
D0	PLL3G_LDout	Channel #1 PLL status: "0" not locked "1" locked	-
Reg44, 0x2C			
D7–D0	Service settings	Do not change	"01110100"
Reg45, 0x2D			
D7–D0	Service settings	May change its state	-
Reg46, 0x2E			
D7–D1	Unused	Unused	"0000000"
D0	PLL3G_SAS_EXE	Channel #1 PLL subband autoselection system execute: "0" finished "1" start (reset to "0" automatically when finished)	"0"
Reg47, 0x3F			
D7–D6	Unused	Unused	"00"
D5–D2	Service settings	Do not change	"0110"
D1–D0	PLL2G_CDiv<9:8>	Channel #2 C-divider ratio (refer to formula in section 7.10 for F_{CLK} calculation): "0000000000" unused … unused "0000010100" unused "0000010101" 21 … with step of 1 "1111111111" 1023 **Note:** Available if PLL2G_CDIV_EN = "1"	"00"
Reg48, 0x30			
D7–D0	PLL2G_CDiv<7:0>	Continue. Refer to Reg47 <D1–D0>.	"01000000"

Bit number	Description		Default
Reg49, 0x31			
D7–D0	Service settings	Refer to section 7.6.	“00001100”
Reg50, 0x32			
D7–D2	Unused	Unused	“000000”
D1–D0	PLL2G_NDiv<9:8>	Channel #2 N-divider ratio (refer to formula in section 7.5 for F_{LO} calculation): “0000000000” unused … unused “0000101001” unused “0000101010” 42 … with step of 1 “1111111111” 1023	“00”
Reg51, 0x33			
D7–D0	PLL2G_NDiv<7:0>	Continue. Refer to Reg50 <D1–D0>.	“10001111”
Reg52, 0x34			
D7–D0	PLL2G_DSM_N<23:16>	Channel #2 N-divider fractional ratio (F-divider). Refer to formula in section 7.5 for F_{LO} calculation. 0_{dec} N-divider ratio is integer other N-divider ratio is fractional PLL3G_DSM_N<23:0>=fraction*2^{24}	“00000000”
Reg53, 0x35			
D7–D0	PLL2G_DSM_N<15:8>	Continue. Refer to Reg52 <D7–D0>.	“00000000”
Reg54, 0x36			
D7–D0	PLL2G_DSM_N<7:0>	Continue. Refer to Reg52 <D7–D0>.	“00000000”
Reg55, 0x37			
D7–D6	Unused	Unused	“00”
D5–D0	Service settings	Refer to section 7.6.	“011110”
Reg56, 0x38			
D7–D0	Service settings	Refer to section 7.6.	“01101100”
Reg57, 0x39			
D7–D5	Unused	Unused	“000”
D4–D0	Service settings	Refer to section 7.6.	“00000”
Reg58, 0x3A			
D7–D4	Unused	Unused	“0000”
D3	Service setting	May change its state	-
D2–D1	PLL2G_SAS_CMPH PLL2G_SAS_CMPL	Channel #2 VCO voltage comparator status: “00” valid “01” lower threshold exceeded (oscillation frequency is too low) “10” upper threshold exceeded (oscillation frequency is too high) “11” unused	-
D0	PLL2G_LDout	Channel #2 PLL status: “0” not locked “1” locked	-
Reg59, 0x3B			
D7–D0	Service settings	Do not change	“01110100”
Reg60, 0x3C			
D7–D0	Service settings	May change its state	-
Reg61, 0x3D			
D7–D1	Unused	Unused	“0000000”
D0	PLL2G_SAS_EXE	Channel #2 PLL subband autoselection system execute: “0” finished “1” start (reset to “0” automatically when finished)	“0”

Bit number	Description		Default
Reg62, 0x3E			
D7–D3	Unused	Unused	“00000”
D2-D0	LBI_Lvl<2:0>	Battery level comparator setting: “000” 1.619 V “001” 1.665 V “010” 1.715 V “011” 1.764 V “100” 1.814 V “101” 1.864 V “110” 1.913 V “111” 1.955 V	“010”
Reg63, 0x3F			
D7–D4	Unused	Unused	“0000”
D3–D2	Service settings	Do not change	“01”
D1–D0	CLK_BUF_CC<1:0>	Clock output signal front: “00” 7.7 ns “01” 3.8 ns “10” 2.6 ns “11” 2.0 ns	“10”
Reg64, 0x40			
D7–D0	Service settings	Do not change	“00000000”
Reg65, 0x41			
D7–D4	Unused	Unused	“0000”
D3–D0	Service settings	Do not change	“0000”
Reg66, 0x42			
D7–D2	Service settings	Do not change	“000000”
D1	TEST_GPO1_EN	General purpose output (pin #17): “0” disabled “1” enabled **Note:** Automatically enabled if CLK_OUT<1:0> = “11”.	“0”
D0	TEST_GPO0_EN	General purpose output (pin #18): “0” disabled “1” enabled **Note:** Automatically enabled if CLK_OUT<1:0> = “10” or “11”.	“1”
Reg67, 0x43			
D7	Unused	Unused	“0”
D6–D0	Service settings	Do not change	“0011111”
Reg68, 0x44			
D7–D0	Service settings	Do not change	“11001111”
Reg69, 0x45			
D7–D6	Unused	Unused	“00”
D5–D0	Service settings	Do not change	“011010”
Reg70, 0x46			
D7	Unused	Unused	“0”
D6–D0	Service settings	May change its state	-
Reg71, 0x47			
D7	Unused	Unused	“0”
D6–D0	LPF1_ctr<6:0>	Channel #1 LPF cut-off frequency setting status	-
Reg72, 0x48			
D7	Unused	Unused	“0”
D6–D0	LPF2_ctr<6:0>	Channel #2 LPF cut-off frequency setting status	-

Bit number	Description		Default
Reg73, 0x49			
D7–D3	Unused	Unused	“00000”
D2–D0	rev_gds<2:0>	GDS file revision: “000” 0 “001” 1 “010” 2 – current version “011” 3 “100” 4 “101” 5 “110” 6 “111” 7	-
Reg74, 0x4A			
D7–D0	Service settings	Do not change	“01010101”

5. OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage _____ –0.5…+3.6 V
Maximum input signal level _____ +10dBm
Operating temperature range _____ –40…+85°C
Storage temperature _____ –55…+125°C
Junction temperature _____ +150°C
Soldering temperature _____ +260°C
Thermal resistance (crystal-package) _____ +28 °C/W
Electrostatic discharge rating:

- HBM (pins #3, 12, 17, 18, 19, 20, 21, 22, 32) _____ 500…1000kV
- HBM (except pins #2, 3, 12, 17, 18, 19, 20, 21, 22, 32) _____ 250…500kV
- HBM (pin #2) _____ 125…250kV

5.1. DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{CC_HV} = 1.71 V to 3.6V, V_{CC_LV} = 1.71 V to 1.89V, T_a =–40…+85°C. Typical values are at V_{CC_HV} = 1.8 V, V_{CC_LV} = 1.8 V, T_a =+25°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
High level supply voltage	V_{CC_HV}	@ pin #3	1.71	1.8	3.6	V
Low level supply voltage	V_{CC_LV}	@ pins #2, 4, 8, 11, 12, 23, 25, 29, 30	1.71	1.8	1.89	V
Power consumption	P	Mode 1.1 / Mode 1.2	–	56.9/56.5	–	mW
		Mode 2.1 / Mode 2.2	–	47.2/46.8	–	
		Mode 3.1 / Mode 3.2	–	34.7/34.5	–	
		Mode 4.1 / Mode 4.2	–	24.8/24.6	–	
Standby current	I_{STB}	–	–	0.7	34	uA
Input logic-level high	V_{IH}	–	V_{CC_LV} –0.3	–	V_{CC_LV}	V
Input logic-level low	V_{IL}	–	0	–	0.3	V
Output logic-level high	V_{OH}	I_{LOAD} = 100uA	V_{CC_LV} –0.3	–	V_{CC_LV}	V
Output logic-level low	V_{OL}	I_{LOAD} = 100uA	0	–	0.3	V
IFA output DC level	V_{DC_IFA}	–	1.15	1.4	1.75	V
Die temperature measurement range	T_j	–	-40	–	100	°C
Die temperature measurement resolution	ΔT_j	–	–	1.67	–	°C
Die temperature measurement accuracy	γT_j	–	–	±10	–	°C
TCXO supply voltage	V_{CC_TCXO}	Maximum I_{LOAD}=5mA	1.65	1.8	–	V
LNA supply voltage	V_{CC_LNA}	Maximum I_{LOAD}=25mA	1.65	1.8	–	V
Active antenna supply voltage	V_{AA}	Preset 1	–	1.8	–	V
		Preset 2	–	2.4	–	
		Preset 3	–	2.7	–	
		Preset 4	–	3.0	–	
Active antenna supply voltage drop	ΔV_{AA}	V_{CC_HV}=V_{AA}=1.8V, I_{LOAD}=10mA	–	55	–	mV
		V_{CC_HV}=V_{AA}=3.0V, I_{LOAD}=10mA	–	56	–	
Active antenna detection current	I_{AA_C}	Tunable. Preset 5	–	1.5	–	mA
Short-circuit protection current	I_{AA_SH}	Tunable. Preset 5	–	18	–	mA

Modes:
1. 2 channels @ splitter input (2 combinations of L1 and L2/L3/L5 bands @ PLL #1, #2)
2. 2 channels @ mixer inputs (2 combinations of L1 and L2/L3/L5 bands @ PLL #1, #2)
3. 1 channel @ splitter input (L1 or L2/L3/L5 band @ PLL #1 or PLL #2)
4. 1 channel @ mixer input (L1 or L2/L3/L5 band @ PLL #1 or PLL #2)

* .1 analog differential output
* .2 2-bit ADC output

5.2. AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{CC_HV} = 1.71 V to 3.6V, V_{CC_LV} = 1.71 V to 1.89V, T_a =–40…+85°C. Typical values are at V_{CC_HV} = 1.8 V, V_{CC_LV} = 1.8 V, T_a =+25°C, unless otherwise specified.

Parameter	Symbol	Condition			Value min	Value typ	Value max	Unit
Overall								
Input frequency range	F_{IN}	Channel #1 @ L1 band			1530	–	1620	MHz
		Channel #2 @ L2, L3, L5 band			1160	–	1300	
Total maximum power gain	G_P	Reffered to splitter input		L1 band	–	78	–	dB
				L2/L3/L5 band	–	80	–	
		Reffered to mixer input		L1 band	–	80	–	
				L2/L3/L5 band	–	82	–	
Noise figure	NF	G_{IF} > 45	Reffered to splitter input	L1 band	–	12	–	dB
				L2/L3/L5 band	–	10	–	
			Reffered to mixer inputs	L1 band	–	10	–	
				L2/L3/L5 band	–	8	–	
1dB compression point	P1dB	G_{IF}=min	Reffered to splitter input	L1 band	–	-40	–	dBm
				L2/L3/L5 band	–	-41	–	
			Reffered to mixer inputs	L1 band	–	-40	–	
				L2/L3/L5 band	–	-41	–	
Splitter&Mixer&Polyphase filter								
RF power gain	G_{RF}	Reffered to splitter input		L1 band	–	10	–	dB
				L2/L3/L5 band		12		
		Reffered to mixer input		L1 band	–	12	–	
				L2/L3/L5 band		14		
Image rejection	IR	–			–	30	–	dB
Input VSWR	$VSWR_{RF}$	With matching circuit. 50Ohm	Reffered to splitter input	L1 band	–	1.6	1.9	–
				L2/L3/L5 band	–	2.2	2.3	
			Reffered to mixer input	L1 band	–	1.6	3.0	
				L2 band	–	1.6	3.4	
				L3 band	–	2.7	–	
				L5 band	–	1.7	2.3	
				E6 band	–	1.5	–	
LPF&IFA								
Output frequency range	F_{OUT}	–			3	–	20	MHz
LPF 3dB cut-off frequency	F_{CUT_LPF}	Channel #1 / Channel #2			4	–	19/20	MHz
IF minimum power gain	G_{IF_MIX}	R_{IN_IF}=2kOhm, R_{OUT_IF}=2kOhm			–	0	–	dB
IF maximum power gain	G_{IF_MAX}	R_{IN_IF}=2kOhm, R_{OUT_IF}=2kOhm			–	68	–	dB
IF AGC range	ΔG_{IF}	–			–	68	–	dB
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	V_{p-p}	–			180/480	200/480	220/530	mVp-p
Stopband attenuation	S_A	F_{CUT_LPF} = default		F = 2×F_{CUT_LPF}	–	13	–	dB
				F = 3×F_{CUT_LPF}	–	20	–	
Group time delay ripple	ΔT_{GD}	–			–	TBD	–	ns
ADC								
Resolution	R_{ADC}	–			–	2	–	bit
Output logic-level high	V_{OH_ADC}	I_{LOAD} = 0mA/2mA			–	1.8/1.7	–	V
Synthesizer								
Reference frequency	F_{REF}	–			10	16.368	40	MHz
Reference signal input level	REF_{IN}	Sine or triangle wave			0.6	–	1.0	Vp-p
PFD frequency range					5	16.368	40	MHz

Parameter	Symbol	Condition		Value			Unit
				min	typ	max	
LO frequency range	F_{LO}	Channel #1 @ L1 band		1550	–	1600	MHz
		Channel #2 @ L2, L3, L5 band		1150	–	1280	
VCO frequency range	F_{VCO}	Channel #1 @ L1 band		3100	–	3200	MHz
		Channel #2 @ L2, L3, L5 band		2300	–	2560	
VCO to PFD frequency integer-valued division ratio	N	–		–	10	–	bit
VCO to PFD frequency fraction-valued division resolution	F	–		–	24	–	bit
VCO to CLK frequency integer-valued division ratio	C	–		–	10	–	bit
TCXO to PFD frequency integer-valued division ratio	R	–		–	1	2	–
LO phase noise	PN_{LO}	Integer-N mode, F_{PFD}=16.368MHz, F_{LO}=1571.328 MHz	At 10kHz offset	–	–94.7	–	dBc/Hz
			At 100kHz offset	–	–94.0	–	
			At 1MHz offset	–	–115.5	–	
		Integer-N mode, F_{PFD}=16.368MHz, F_{LO}=1170.312 MHz	At 10kHz offset	–	–97.9	–	
			At 100kHz offset	–	–97.2	–	
			At 1MHz offset	–	–122.8	–	
LO RMS jitter	J_{RMS}	Integer-N mode, Integrated BW=100MHz, F_{PFD}=16.368MHz	L1 band	–	1.7	–	ps
			L2, L3, L5 band	–	1.3	–	
Clock frequency	F_{CLK}	–		10	16.368	50	MHz
Output logic-level high at CMOS clock output	V_{OH_CLK}	C_{LOAD}=5pF		1.7	1.8	1.9	V
Output logic-level low at CMOS clock output	V_{OL_CLK}	–		–	–	0.2	V

6. TYPICAL CHARACTERISTICS

6.1. S-PARAMETERS

Please, open the attachment of the datasheet to download files with S-parameters. File names are given below.

Test conditions: V_{CC_HV} = 1.8 V, V_{CC_LV} = 1.8 V, T_a =+25°C. The effects of the test fixture have been de-embedded up to the pins of the device.

File name	Parameter	Input pin	Frequency range
NT1062_SPL_IN.txt	S11	#32	L1, L2, L3, L5 bands
NT1062_MIX1_IN.txt	S11	#27	L1 band
NT1062_MIX2_IN.txt	S11	#6	L2, L3, L5 bands

In order to upload files to different RF design environments or any software for viewing Touchstone (SnP) format their type should be changed to .s1p.

Typical S-parameters are provided “as they are” and with no warranty of any kind expressed or implied, including warranties of merchantability and fitness for a particular purpose.

7. APPLICATION NOTES

7.1. START UP PROCEDURE

NT1062 wakes up in standby mode: both channels and clock output are disabled. In order to activate NT1062 one of the IC operating modes should be selected.

7.2. REFERENCE FREQUENCY (TCXO) CONFIGURATION

NT1062 is preconfigured to operate with 16.368MHz reference frequency source (TCXO). If another reference frequency will be used, refer to Reg3 D[5–0] and select frequency range to which required reference frequency belongs.

NT1062 is able to supply external TCXO with 1.8V via pin #12 in any active mode. TCXO supply option may be disabled in Reg6 D[5]. If IC mode was changed or IC was activated after standby, TCXO supply should be manually disabled if not needed.

7.3. IC OPERATING MODE CONFIGURATION

Channel #1 is intended to operate in L1 band, channel #2 – in L2/L3/L5 band.

NT1062 is activated by selecting IC operating mode in Reg2 D[2–0]. Input RF signal can be applied to separate mixers inputs (if Reg2 D[2–00] = “001”, “010”, “011”) or to splitter input (if Reg2 D[2–0] = “101”, “110”, “111”).

NT1062 is able to supply external LNAs with 1.8V via pins #4 and #29 when Reg2 D[2–0] is set to “001”, “010” or “011”.

When Reg2 D[2–0] is set to “101”, “110” or “111” NT1062 will provide supply voltage (1.8V, 2.4V, 2.7V or 3.0V according to Reg13 D[1–0]) for external active antenna via pin #2. Active antenna supply option may be disabled in Reg7 D[5]. If IC mode was changed or IC was activated after standby, active antenna supply should be manually disabled if not needed.

7.4. SYSTEM STATUS

Common cumulative status indicator (AOK) is available in Reg14 D[6]. AOK indicator is configurable, it’s components can be selected in Reg5.

Battery level indicator is available in Reg14 D[3] and returns “1” when IC supply voltage is too low. It’s level is configurable and may be changed in Reg62 D[2–0]. Battery level indicator may be disabled by writing “0” to Reg7 D[7]. If IC mode was changed or IC was activated after standby, battery level indicator should be manually disabled if not needed. Write “0” to Reg5 D[5] to excluded it from AOK.

Reference frequency indicator is available in Reg14 D[4] and returns “1” when TCXO signal is too low or is absent.

7.5. PLL RECONFIGURATION

NT1062 has the following presettings:

- PLL #1 is set to feed channel #1 with LO = 1571.328MHz @ F_{REF} = 16.368MHz
- PLL #2 is set to feed channel #2 with LO = 1170.312MHz @ F_{REF} = 16.368MHz

PLL #1 is intended to operate in L1 band, PLL #2 – in L2/L3/L5 band.

In order to reconfigure PLL #1 and PLL #2 the following procedure is recommended:

- make sure that applied reference frequency belons to selected frequency range in Reg3 D[5–0] and status in Reg14 D[4] is valid;
- choose R, N, F using the formula $F_{LO} = \frac{F_{REF} \times N}{2R}$ or $F_{LO} = \frac{F_{REF} \times (N + F/2^{24})}{2R}$;
- write R value to Reg2 D[7] for channel #1 PLL / Reg2 D[6] for channel #2 PLL;
- write N value to Reg35 D[1–0] + Reg36 D[7–0] for channel #1 PLL / Reg50 D[1–0] + Reg51 D[7–0] for channel #2 PLL;
- if F ≠ 0, enable delta-sigma modulator (DSM) in Reg8 D[1] for channel #1 PLL / Reg9 D[1] for channel #2 PLL and write F value to Reg37 D[7–0] + Reg38 D[7–0] + Reg39 D[7–0] for channel #1 PLL / Reg52 D[7–0] + Reg53 D[7–0] + Reg54 D[7–0] for channel #2 PLL;
- execute tuning procedure in Reg46 D[0] for channel #1 PLL / Reg61 D[0] for channel #2 PLL.

If reference frequency was changed, it is necessary to repeat described procedure and execute tuning procedure for each PLL.

PLL lock indicator is available in Reg43 D[0] for channel #1 / Reg58 D[0] for channel #2.

Crossing of VCO voltage comparator lower threshold will be indicated by Reg43 D[1] for channel #1 / Reg58 D[1] for channel #2. Crossing of VCO voltage comparator upper threshold will be indicated by Reg43 D[2] for channel #1 / Reg58 D[2] for channel #2.

7.6. PLL LOOP FILTER ADJUSTMENT

PLL loop filter should be adjusted to get better LO frequency phase noise if PFD frequency differs from default value. The following registers values should be written to NT1062 depending on PFD frequency value:

Channel #1:

- $F_{PFD} \leq 25$MHz
  - Reg34 0x0C (in integer-N mode) / 0x0D (in fractional-N mode)
  - Reg40 0x16
  - Reg41 0x89
  - Reg42 0x00
- $F_{PFD} > 25$MHz
  - Reg34 0x0C (in integer-N mode) / 0x0D (in fractional-N mode)
  - Reg40 0x1E
  - Reg41 0x2D
  - Reg42 0x00

Channel #2:

- $F_{PFD} \leq 25$MHz
  - Reg49 0x0C (in integer-N mode) / 0x0D (in fractional-N mode)
  - Reg55 0x1E
  - Reg56 0x6C
  - Reg57 0x00
- $F_{PFD} > 25$MHz
  - Reg49 0x0C (in integer-N mode) / 0x0D (in fractional-N mode)
  - Reg55 0x1F
  - Reg56 0x2F
  - Reg57 0x00

Execute PLL tuning procedure after loop filter adjustment.

Values must be written each time after power up.

If PLL loop filter was adjusted for not default conditions, default values must be overwritten to return to default state.

7.7. CHANNEL MODE CONFIGURATION

Each real channel with image rejection option may be individually configured to pass upper or lower sideband of configurable width. Channel sideband may be selected in Reg17 D[6] for channel #1 and Reg19 D[6] for channel #2.

LPF cut-off frequency may be changed in Reg25 D[6–0] for channel #1 and Reg30 D[6–0] for channel #2 after active mode initiation.

LPF cut-off frequency status is available in Reg71 D[6–0] for channel #1 and Reg72 D[6–0] for channel #2.

7.8. IF GAIN CONTROL

IF gain control system starts into the auto operation mode with 2-bit ADC IF outputs. You can change digital detector threshold with respect to sinewave signal with Reg22 D[1–0] + Reg23 D[7–0] for channel #1 and Reg27 D[1–0] + Reg28 D[7-0] for channel #2.

To enable manual mode write “0” to Reg21 D[0] for channel #1 and Reg26 D[0] for channel #2. Then you can change IF gain value manually by setting a corresponding value with Reg22 D[1–0] + Reg23 D[7–0] for channel #1 and Reg27 D[1–0] + Reg28 D[7–0] for channel #2.

When output data interface is analog and IF AGC system is enabled, refer to Reg24 D[1-0] to change IFA output amplitude for channel #1, Reg29 D[1-0] – for channel #2.

7.9. OUTPUT DATA INTERFACE CONFIGURATION

After power up NT1062 is preconfigured to 2-bit ADC output data interface. However, there is an option to set up analog differential outputs by writing “0” to Reg 21 D[3] for channel #1 and to Reg 26 D[3] for channel #2.

IFA digital detector must be manually disabled in analog mode by writing “0” to Reg21 D[2] for channel #1 and Reg 26 D[2] for channel #2. Do not forget to enable IFA digital detector when returning to 2-bit ADC mode.

2-bit ADCs can operate in synchronous (set by default) or asynchronous mode. In asynchronous mode 2-bit ADCs act as voltage level comparators and clock is not required. Asynchronous mode is useful when several NT1062 ICs are used at the same time, in this case IF output data should be synchronized externally with single clock signal. Make sure that processor is placed close to each NT1062 ICs and their output load is within acceptable limits. ADC mode can be changed from default setting by writing “0” to Reg2 D[4] for channel #1 and Reg2 D[3] for channel #2. If only one NT1062 IC is used, then synchronous mode is recommended.

7.10. CLK FREQUENCY CONFIGURATION

CLK signal is intended for clocking internal 2-bit ADCs in synchronous mode as well as clocking external correlator engine. CLK signal can be generated from LO frequency either from PLL #1 or PLL #2 or is taken from external TCXO.

TCXO pass-through mode is set by default (Reg2 D[5] is set to “1”), C-dividers are disabled in PLL #1 and PLL #2.

Follow the procedures to generate CLK signal from PLL #1 or PLL #2:

- disable TCXO pass-through mode – write "0" to Reg2 D[5];
- calculate C-divider value according to the formula: $F_{CLK} = F_{LO}/C$;
- enable C-divider of PLL #1 or PLL #2 – write "1" to Reg8 D[0] or Reg9 D[0];
- write C-divider value to Reg32 D[1–0] + Reg33 D[7–0] / Reg47 D[1–0] + Reg48 D[7–0].

Clock output may be disabled to save power consumption if output data interface is analog or 2-bit ADC mode is asynchronous: write "0" to Reg6 D[7] after changing IC mode. If IC mode was changed or IC was activated after standby,clock output buffer should be manually disabled if not needed.

7.11. CLOCK OUTPUT TYPE CONFIGURATION

Clock output type is CMOS. Refer to Reg63 D[1–0] to adjust clock output signal front.

CMOS clock signal is available on pin #17. In pair with CMOS clock signal AOK status or general purpose signal (GPO) may be taken from pin #18. Reg4 D[1–0] must be set to appropriate mode depending on selected option.

Choosing frequency plan and clock frequency pay attention to appearing of interferences at the RF input pins and then down converting to IF band. These interferences are caused by CLK signal harmonics and allocated frequencies can be calculated as $F_{jam} = N \times F_{CLK}, N = 1,2,3, \dots$.

7.12. ACTIVE ANTENNA DETECTOR

Active antenna detector is intended to detect whether active antenna is connected to splitter input and to limit active antenna supply voltage if its current is too high.

Active antenna current consumption setting may be changed in Reg13 D[4–2].

If active antenna current is four or more times lower than selected setting, active antenna connection status will be fail (connection indicator available in Reg14 D[0]).

If active antenna current is two or more times higher than selected setting, then output voltage be reduced to 0V.

Active antenna supply voltage output is configurable and may be changed in Reg13 D[1–0]. If active antenna detector input level is not enough to provide output voltage, then indicator in Reg14 D[2] will return "1".

Active antenna detector may be disabled by writing "0" to Reg7 D[5] after changing IC mode.

7.13. TEMPERATURE MEASUREMENT PROCEDURE

Temperature measurement is done once upon request to Reg10 D[0] by setting "1" (auto reset to "0" when finished) and result will be stored in Reg11 D[1–0] + Reg12 D[7–0] after procedure is finished until next execution. Temperature measurement procedure status is available in Reg11 D[2].

7.14. OPERATION EXAMPLES

7.14.1. CONFIGURATION SETS #1, 3

General settings:		
Reference frequency	16.368 MHz	
IC mode	NT1062_1_ConfigSet1.X	NT1062_1_ConfigSet3.X
	Ch#1 EXT LNA + Ch#2 EXT LNA	Ch#1 SPL + Ch#2 SPL
CLK settings:		
CLK frequency source	TCXO pass-through	
CLK frequency	16.368 MHz	
CLK type	CMOS	
CLK amplitude	1.8V	
PLL settings:		
F_{LO} PLL #1	1571.328 MHz	
F_{LO} PLL #2	1170.312 MHz	
Channel settings:		
Channel #1 sideband	Upper sideband (GAGAN L1, GPS L1, QZSS L1)	
Channel #2 sideband	Upper sideband (GAGAN L5, NavIC L5)	
Channel #1 IF passband	5.2MHz	
Channel #2 IF passband	7.2MHz	
GC mode:		
Channel #1	IF auto	
Channel #2	IF auto	
Output data interface:	NT1062_1_ConfigSetX.1	NT1062_1_ConfigSetX.2
Channel #1	2-bit ADC	analog differential
Channel #2	2-bit ADC	analog differential
ADC output logic-level high	1.8V	-
ADC type	Synchronous	-

7.14.2. CONFIGURATION SET #2

General settings:		
Reference frequency	16.368 MHz	
IC mode	Ch#1 EXT LNA + Ch#2 EXT LNA	
CLK settings:		
CLK frequency source	TCXO pass-through	
CLK frequency	16.368 MHz	
CLK type	CMOS	
CLK amplitude	1.8V	
PLL settings:		
F_{LO} PLL #1	1571.328 MHz	
F_{LO} PLL #2	1223.508 MHz	
Channel settings:		
Channel #1 sideband	Upper sideband (GAGAN L1, GPS L1, QZSS L1)	
Channel #2 sideband	Upper sideband (GPS L2, QZSS L2)	
Channel #1 IF passband	5.2MHz	
Channel #2 IF passband	5.2MHz	
GC mode:		
Channel #1	IF auto	
Channel #2	IF auto	
Output data interface:	NT1062_1_ConfigSet2.1	NT1062_1_ConfigSet2.2
Channel #1	2-bit ADC	analog differential
Channel #2	2-bit ADC	analog differential
ADC output logic-level high	1.8V	-
ADC type	Synchronous	-

NT1062_1_2_ConfigSetX.X_vX.txt files are attached. In order to use attached file under GUI its type should be changed to .hex.

7.15. PCB LAYOUT RECOMMENDATIONS

7.15.1. RECOMMENDED LAND PATTERN

NT1062 is easy-to-use and easy-to-implement solution where no special layout tricks required. Although common RF related layout techniques and information given below are recommended not to be ignored.

1. Analog power domain separated from digital domain is recommended to be allocated.
2. EMI-RFI shielding is highly recommended above NT1062 and related stuff.
3. Channels input wave impedance should be 50Ohm for MIX1_IN, MIX2_IN and SPL_IN (traces marked in pink color).
4. Lines between elements of matching network circuits and NT1062 input pins should be as short as possible (traces marked in purple color).
5. Channels #1 and #2 output wave differential impedance can be in the range from 100Ohm to 2kOhm for analog output data interface (traces marked in light green color).

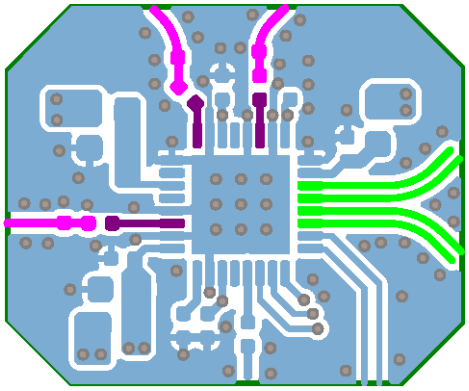


Figure 7.1: Recommended land pattern QFN32: basic application schematic

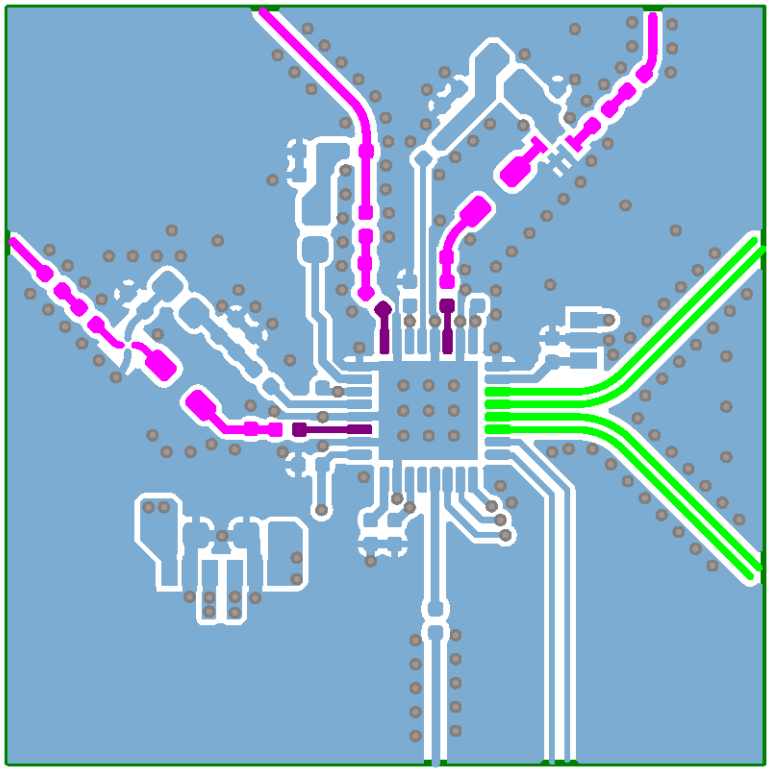


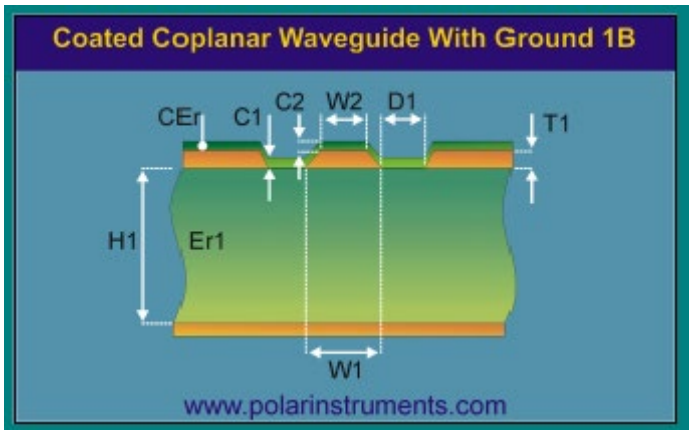
Figure 7.2: Recommended land pattern QFN32: enhanced application schematic

7.15.2. STACK UP

FR4: Core HighTg 1.08mm, PrePreg 7628-45

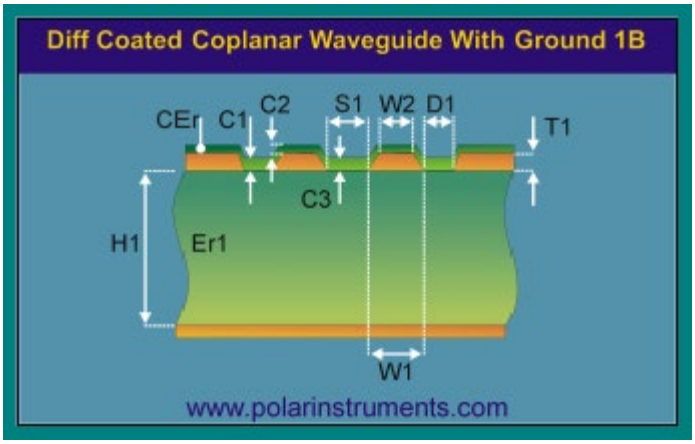
#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder_Mask	Solder Mask		0,025mm	3,6
	Top Surface Finish	Nickel, Gold	Surface Finish		0,02mm	
1	Layer 1		Signal	1/3oz	0,012mm	
	PP7628-45	Pre-preg	Prepreg		0,18mm	4,4
2	Layer 2		Signal	1oz	0,035mm	
	HighTg 1.08mm 35um/35um	Core	Core		1,08mm	4,4
3	Layer 3		Signal	1oz	0,035mm	
	PP7628-45	Pre-preg	Prepreg		0,18mm	4,4
4	Layer 4		Signal	1/3oz	0,012mm	
	Bottom Surface Finish	Nickel, Gold	Surface Finish		0,02mm	
	Bottom Solder	Solder Resist	Solder Mask		0,025mm	3,6
	Bottom Overlay		Overlay			

Figure 7.3: Layer stack manager example



Substrate 1 Height	H1	0,1800
Substrate 1 Dielectric	Er1	4,4000
Lower Trace Width	W1	0,3100
Upper Trace Width	W2	0,2980
Ground Strip Separation	D1	0,3000
Trace Thickness	T1	0,0120
Coating Above Substrate	C1	0,0200
Coating Above Trace	C2	0,0200
Coating Dielectric	CEr	3,5000
Impedance	Zo	49,76

Figure 7.4: 50 Ohm traces calculation example



Substrate 1 Height	H1	0,1800
Substrate 1 Dielectric	Er1	4,4000
Lower Trace Width	W1	0,2500
Upper Trace Width	W2	0,2380
Trace Separation	S1	0,2500
Ground Strip Separation	D1	0,3000
Trace Thickness	T1	0,0120
Coating Above Substrate	C1	0,0200
Coating Above Trace	C2	0,0200
Coating Between Traces	C3	0,0200
Coating Dielectric	CEr	3,5000
Differential Impedance	Zdiff	100,44

Figure 7.5: 100 Ohm differential traces calculation example

8. PACKAGE INFORMATION

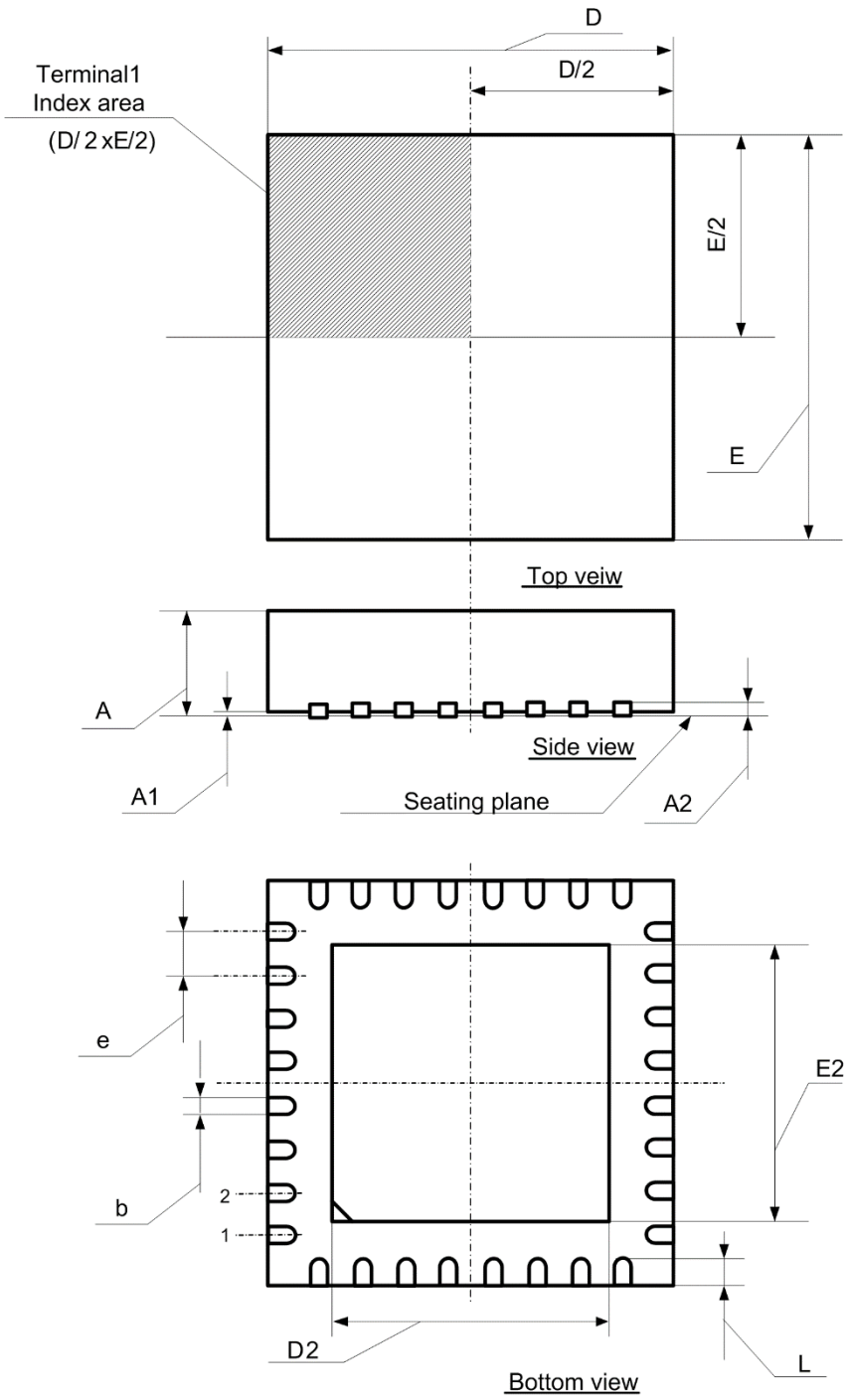


Figure 8.1: NT1062.1.2 QFN32 5mm×5mm package

Table 8.1: Package QFN32 5mm×5mm dimension

Unit	A	A1	A2	b	D	D2	E	E2	e	L
min, mm	0.70	0.00	0.203 REF	0.18	5.00 DSC	3.45	5.00 DSC	3.45	0.50 DSC	0.35
typ., mm	0.75	0.02		0.25		3.50		3.50		0.40
max, mm	0.80	0.05		0.30		3.55		3.55		0.45

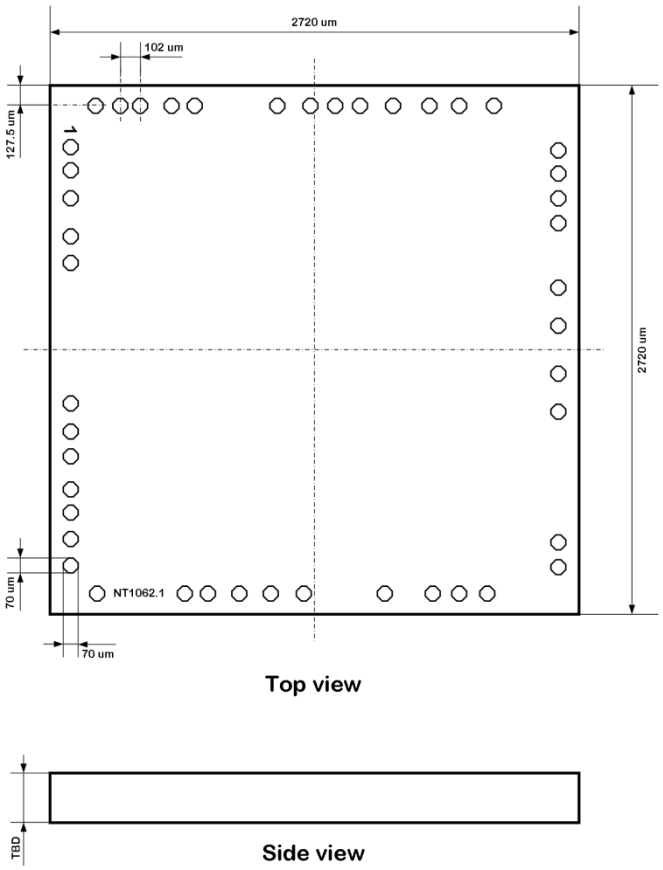


Figure 8.2: NT1062.1.2 bare die drawing

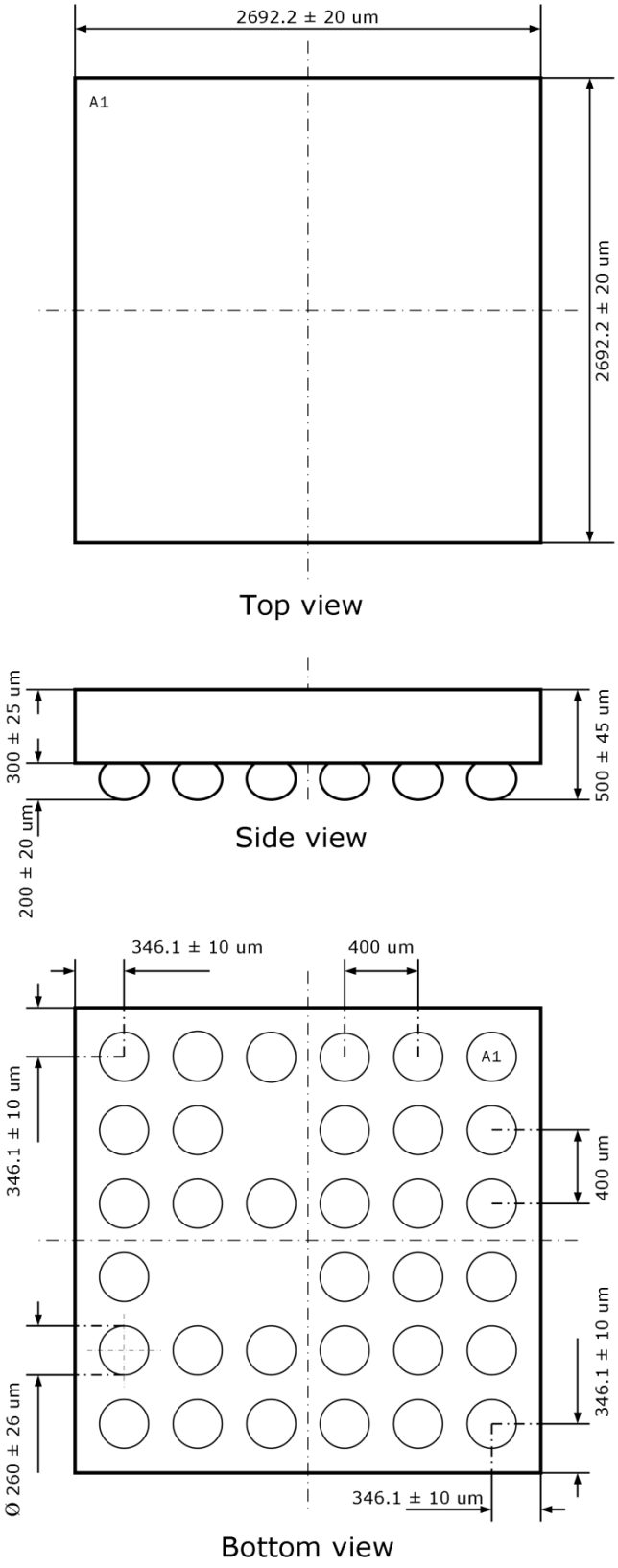


Figure 8.3: NT1062.1.2 WLCSP drawing