

4-Channel GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS S/L1/L2/L3/L5 band Low Power RF Front-End IC

1. RECOMMENDED SETTINGS

Tables below provide recommended values to be written to NT1068.22 registers to achieve specified performance. Recommended values are already included into configuration examples that are part of the evaluation kit documentation delivery. Detailed information about chip parameters and configuration are given in NT1068.22 datasheet and in the manual for evaluation kit.

1.1. GENERAL RECOMMENDED SETTINGS

For each application, please include recommended values given in [Table 1.1](#).

Table 1.1 NT1068.22 general recommended settings

Register address	Recommended value (hex)
Reg4	00
Reg6	0D
Reg75	88
Reg106	00

1.2. PLL “A” AND PLL “B” RECOMMENDATIONS

1.2.1. Galileo mode

If LO_source=“1” (PLL “A” + PLL “B” mode) and PLL_A_Band<1:0> is set to “10” (L2/L3/L5 for ch#2 (Galileo)), write 0xDC to Reg53.

1.2.2. NavIC mode

If PLL “B” is enabled and PLL_B_Band<1:0> is set to “11” (L1 for ch#3 + L3/L5 for ch#4 (NavIC)), while PLL “A” is disabled, then write 0x4F to Reg114.

1.3. CHANNEL #1 AND CHANNEL #2 PASSBAND

Channel #2 passband (Reg14) should be set \geq Channel #1 passband (Reg21).

1.4. CHANNELS RECOMMENDED SETTINGS

When working with individual RF inputs, add values given in [Table 1.2](#) to the end of your configuration. Some values depend on frequency range (S band, L1 band or L2/L3/L5 band) and need to be written for each channel.

Table 1.2 NT1068.22 per-band recommended settings (for individual RF inputs)

Register address				Recommended value (hex)		
Channel #1	Channel #2	Channel #3	Channel #4	S band	L1 band	L2/L3/L5 band
Reg72	Reg82	Reg90	Reg98	D8	D4	D1
Reg75				88	88	88
	Reg83	Reg91	Reg99	08	08	08
Reg76	Reg84	Reg92	Reg100	9B	9B	9B
Reg77	Reg85	Reg93	Reg101	15	15	15

1.5. SPLITTER INPUT RECOMMENDED SETTINGS

Internal 1-to-n RF splitter (n=1,2,3,4) with configurable channel combination can be used along with separate RF inputs for other channels. In order to work with splitter input, do the following actions:

- 1) Enable desired channels and select splitter mode for each channel dedicated to splitter input. Enabled channels that are not set to splitter mode can be supplied with RF signal via RF#_IN pins.
- 2) Configure PLL according application notes given in [section 7.2](#), [7.3](#) and [7.4](#) of NT1068.22 datasheet.
- 3) After PLL frequency band is selected and tuning system is executed, write values given in [Table 1.3](#).

Table 1.3 NT1068.22 splitter input recommended values

Register address				Recommended value (hex)		
Channel #1	Channel #2	Channel #3	Channel #4	S band	L1 band	L2/L3/L5 band
Reg72	Reg82	Reg90	Reg98	50	50	51
Reg77	Reg85	Reg93	Reg101	15	15	15

If NT1068.22 is then ‘on-fly’ switched back to receive signals through separate RF inputs, write values recommended for individual RF inputs.

1.6. ANALOG DIFFERENTIAL OUTPUTS

- 1) For analog differential outputs @ 200mV or 400mV IF AGC threshold, write values given in [Table 1.4](#). Please also refer to Reg15, Reg22, Reg29 and Reg36 description to check value to be written depending on the selected modes.

Table 1.4 NT1068.22 channel output recommended values @ IF AGC enabled

Register address				Recommended value (hex)
Channel #1	Channel #2	Channel #3	Channel #4	
Reg15	Reg22	Reg29	Reg36	2A
Reg78	Reg86	Reg94	Reg102	4D

- 2) If IFA GC mode is set to manual adjustment, then write values given in [Table 1.5](#). Please also refer to Reg15, Reg22, Reg29 and Reg36 description to check value to be written depending on the selected modes.

Table 1.5 NT1068.22 channel output recommended values @ IF AGC in manual mode

Register address				Recommended value (hex)
Channel #1	Channel #2	Channel #3	Channel #4	
Reg15	Reg22	Reg29	Reg36	22
Reg78	Reg86	Reg94	Reg102	0D

- 3) If output data interface type is 2-bit ADC, then do not write values to Reg78, Reg86, Reg94 and Reg102 after power up.