4-Channel GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS S/L1/L2/L3/L5 band Low Power RF Front-End IC

1. OVERVIEW

NT1068.2 is a four-channel RF Front-End IC for the reception of Global Navigation Satellite System (GNSS) signals (GPS, GLONASS, Galileo, BeiDou, NavIC, QZSS) and also signals of satellite-based augmentation systems like OmniSTAR at all frequency bands in various combinations: S, L1, L2, L3, L5, E1, E5a, E5b, E6, B1, B2, B3. NT1068.2 inherits all the features of NT1065 including pin-to-pin compatibility. The key benefits of NT1068.2 over NT1065 are ability to downconvert signals of S-band and input RF splitter with configurable channel combination. When high performance is not needed (e.g. for tracking mode) NT1068.2 can be 'on-fly' switched to ECO mode to furthermore reduce power consumption. There is a specific configuration to acquire signals of S+L2 bands and L1+L3/L5 bands by single chip. Extended functionality of NT1068.2 allows receiving all Galileo signals (E1, E5a, E5b and E6) or other signal combinations in L1/L2 band and L1+L3+L5 bands. As a benefit one can discover wide possibilities of improving the positioning accuracy down to centimeter range without taking RTK technique. Being a low-power RF FE IC with supply voltage from 1.8 to 3.3V it can be used in various mobile applications for high precision positioning. Each setting, including RF input, output signal frequency bandwidth, AGC options, mirror channel suppression option, etc., can be set for every channel individually. NT1068.2 does also integrate two fully independent frequency synthesizers that have the common reference (TCXO) input making LO signals coherent in terms of frequency. Channel#1 and channel#2 are supplied with common LO signal or two different LO signals generated in PLL "A", while PLL "B" is assigned for channels #3 and #4. For specific applications PLL "B" can be also used to feed channel#1 along with channels #3 and #4, PLL "A" – to feed all four channels with single LO signal.

2. FEATURES

- S, L1, L2, L3, L5 bands single conversion super heterodyne receiver with low-IF architecture
- Four independent configurable channels, each includes preamplifier, image rejection mixer, IF filter, IFA, 2-bit ADC
- 1-to-n RF splitter input (n=2,3,4) that can be used along with separate RF inputs for other channels
- Signal bandwidth up to 33MHz supports GNSS high precision codes such as P-code in GPS or wideband E5 Galileo
- Dual adoptable AGC system (RF + IF) or programmable gain
- High dynamic range with 1dB compression point more than –21dBm
- Analog differential output with two options of voltage swing 0.2/0.47Vp-p and 0.4/0.98Vp-p (sine wave/noise) or 2-bit ADC digital output data (CMOS or LVDS)
- Two independent fully integrated synthesizers with flexible LO and CLK frequencies selection
- Wide range of chip supply voltage (from 1.8V ±5% to 3.3V ±10%)
- Low power consumption (50mW per channel) and power economy mode (45mW per channel)
- Embedded temperature sensor
- SPI interface with easy-to-use register map
- Individual status indicators of main subsystems (available in SPI registers) and cumulative status indicator (AOK, available both as a separate pin and in SPI registers)
- Two form-factors: 5.12×5.2mm WLCSP and 10×10mm QFN88 package

3. APPLICATIONS

- GNSS based positioning systems
- GNSS based goniometric systems
- In-vehicle navigation systems
- GNSS based driverless car systems
- Professional drone

4. DESCRIPTION

4.1. BLOCK DIAGRAM

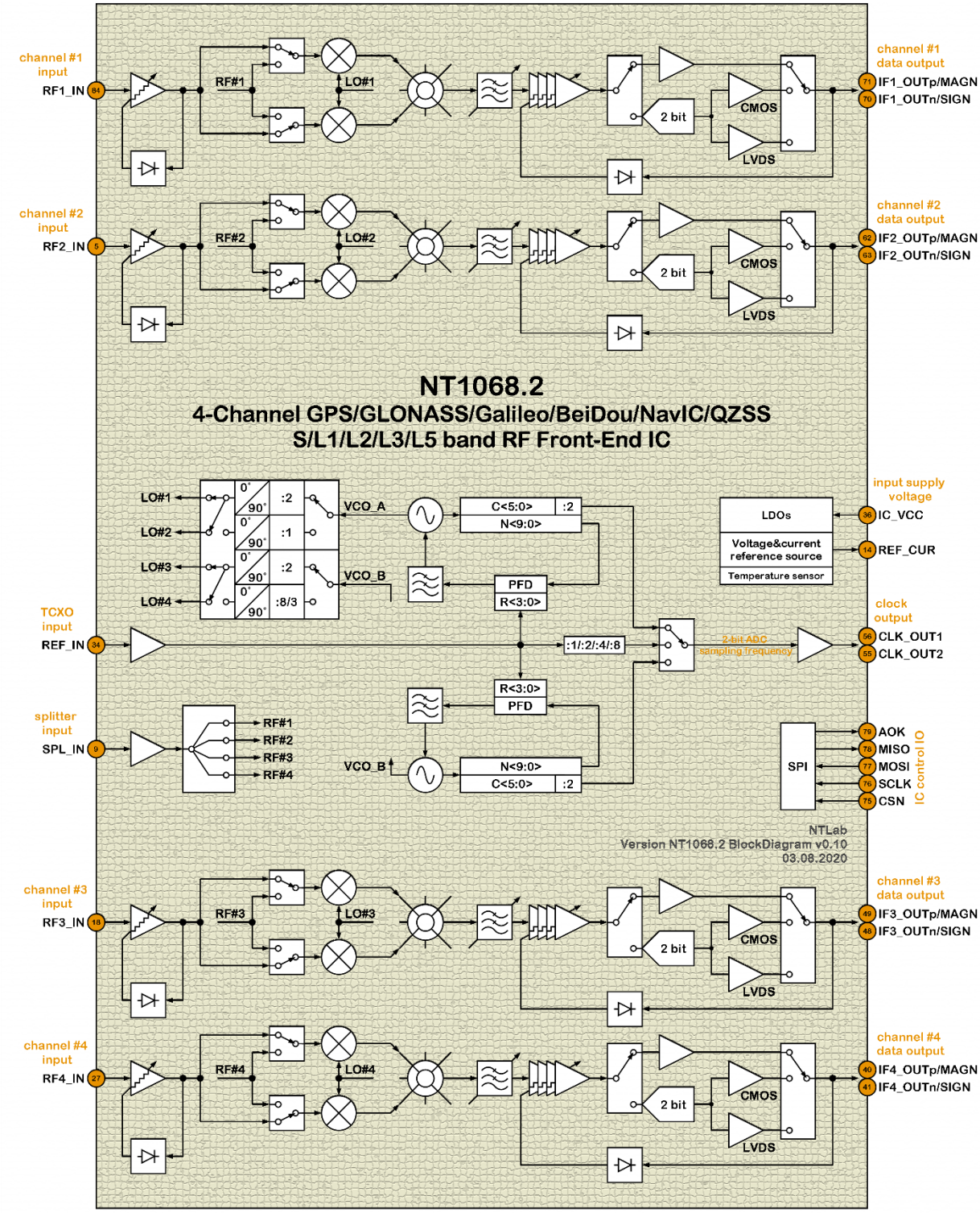


Figure 4.1: NT1068.2 Block diagram

4.2. APPLICATION SCHEMATIC

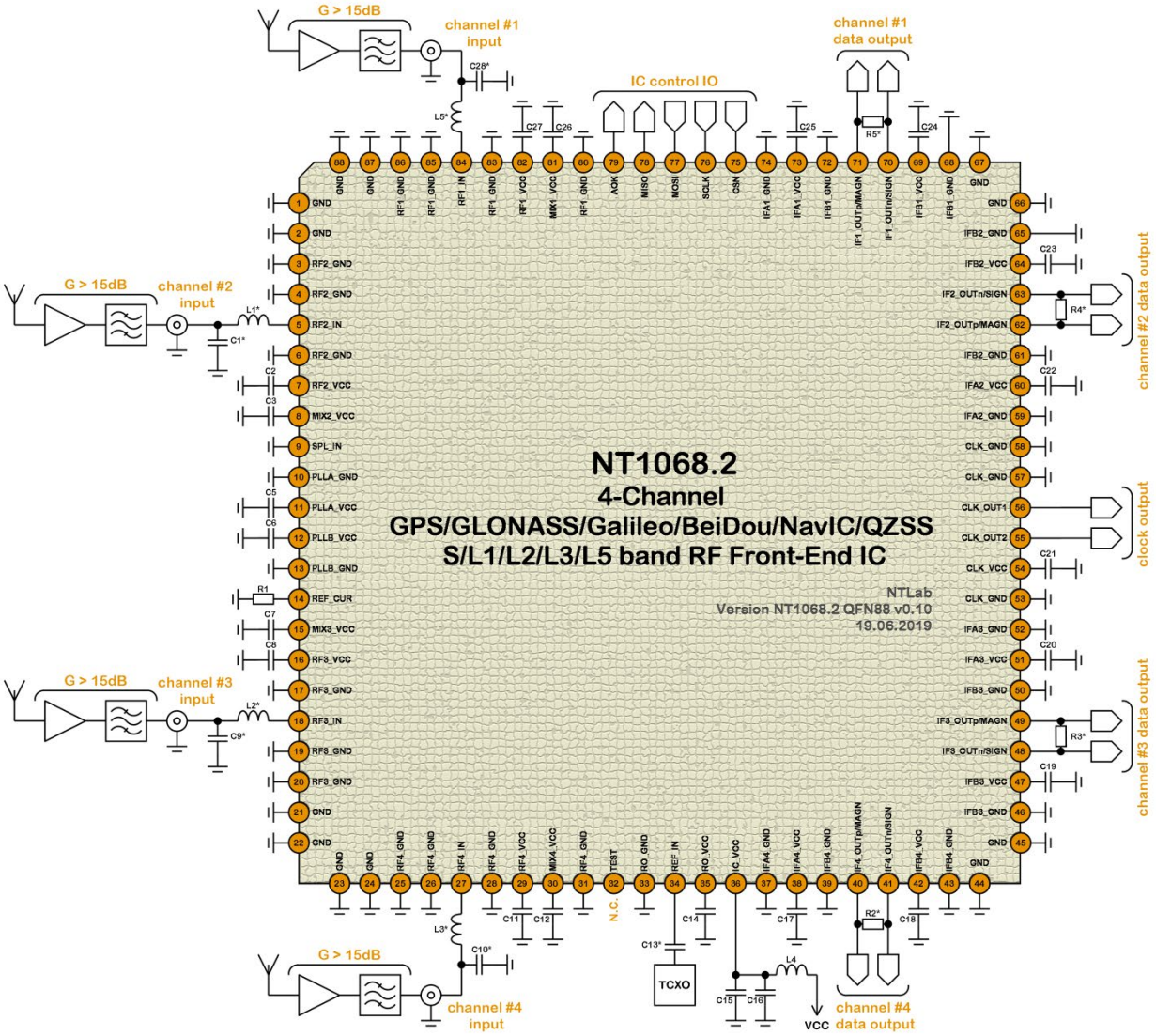


Figure 4.2: NT1068.2 QFN88 application schematic compatible to NT1065

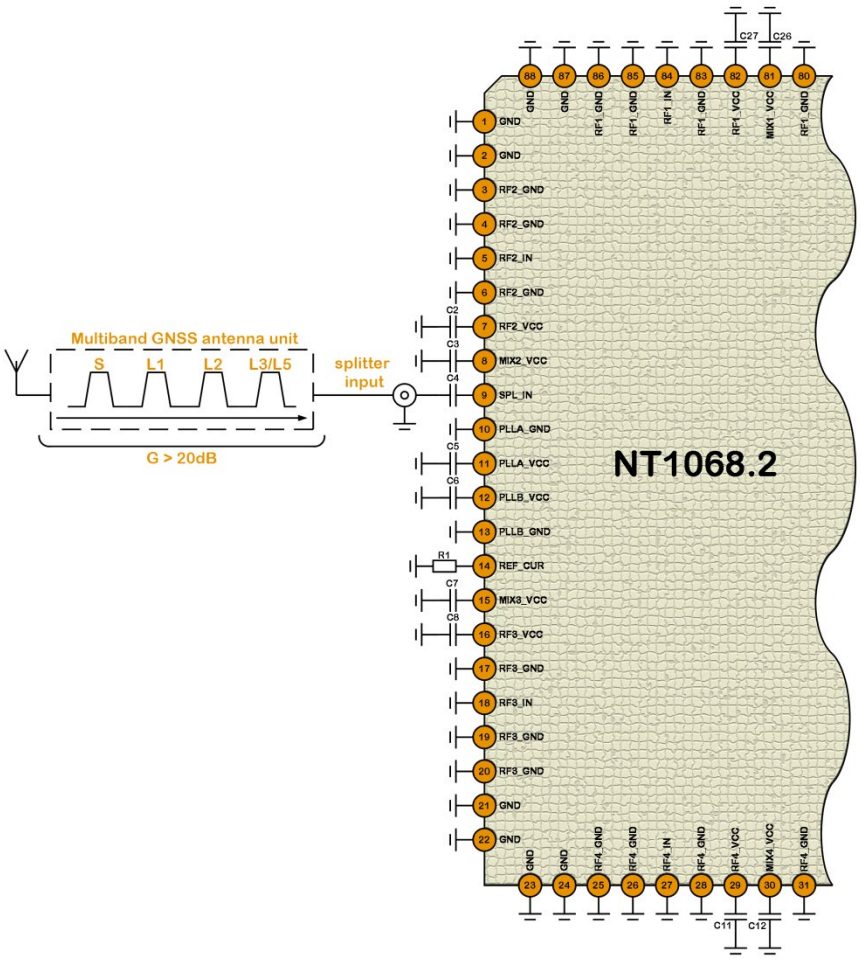


Figure 4.3: NT1068.2 QFN88 multiband GNSS antenna connection to splitter input

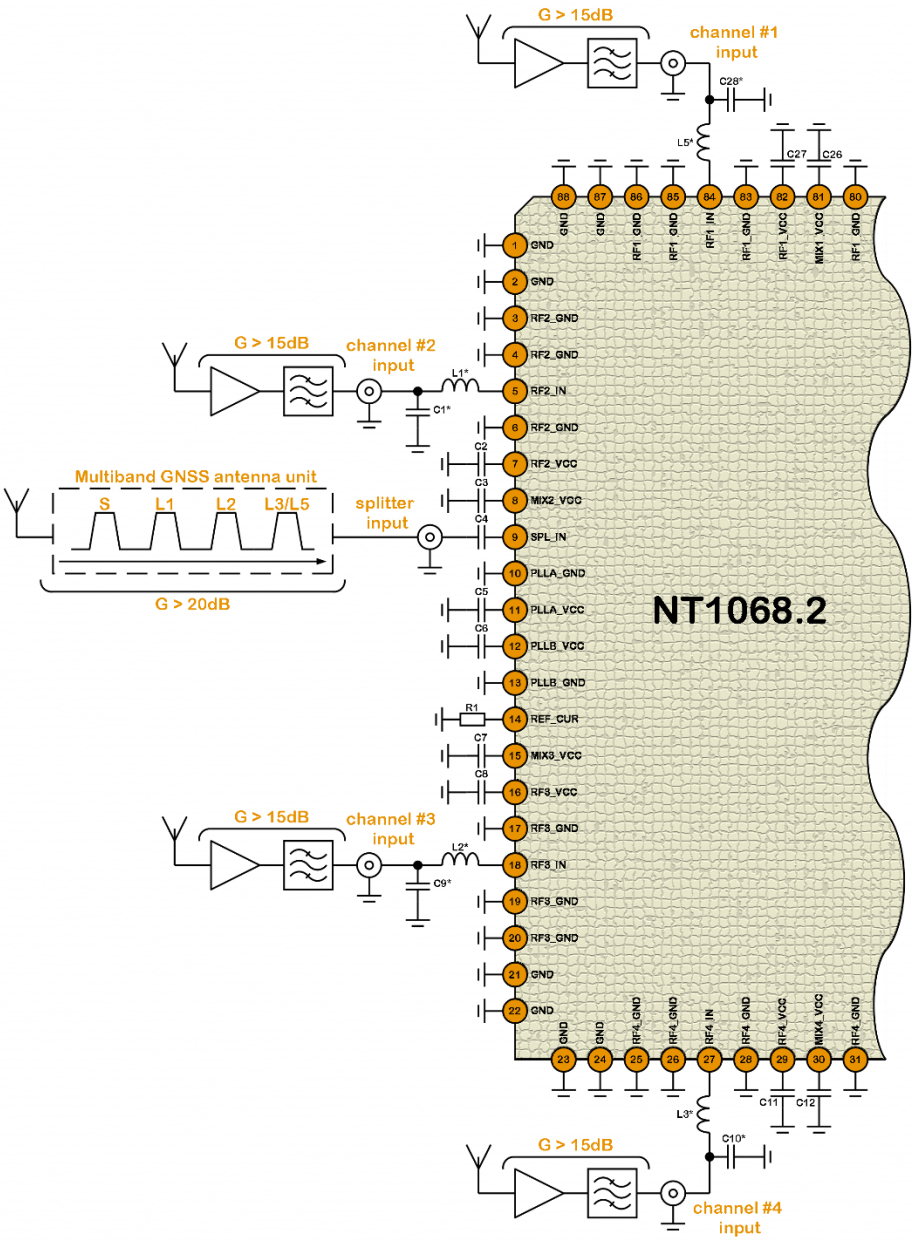


Figure 4.4: NT1068.2 QFN88 multiband GNSS antenna connection to splitter input along with separate RF inputs usage

NT1068.2 can be ‘on-fly’ switched to receive signals either through splitter input or separate RF inputs.

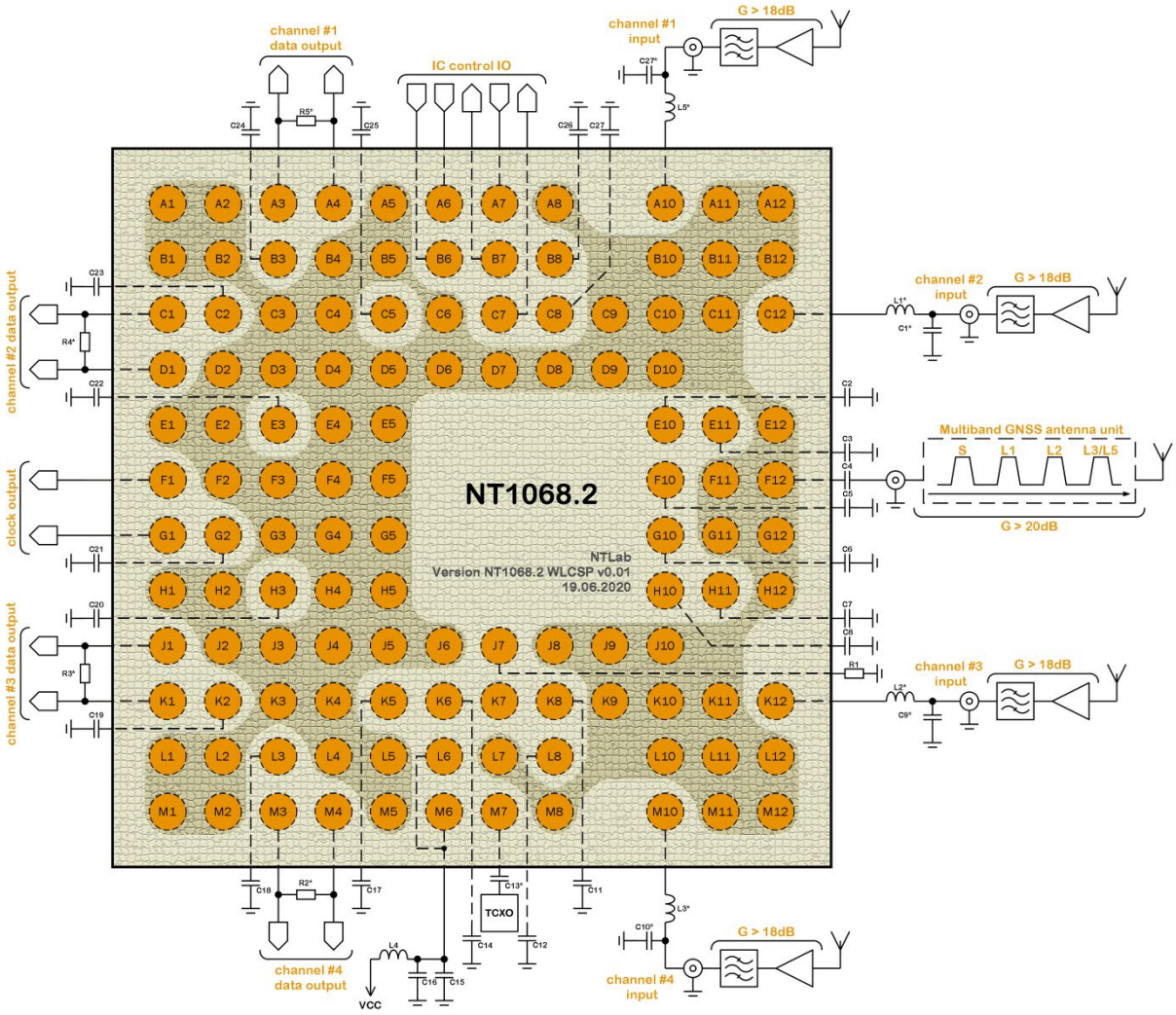


Figure 4.5: NT1068.2 WLCSP (top view) application schematic

Note: WLCSP balls that are not specified on Figure 4.5 (shaded area) except K7 must be connected to the ground.

Table 4.1: External components description

Component	Nominal value	Tolerance	Notes
C1*	3.3pF	±5%	Matching network capacitor for L1 band
	3.3pF	±5%	Matching network capacitor for L2/L3/L5 band
	3.3pF	±5%	Matching network capacitor for E6 band
	2.2pF	±5%	Matching network capacitor for S band
C2	1µF	±20%	Supply voltage filter capacitor
C3	1µF	±20%	Supply voltage filter capacitor
C4	100pF	±20%	DC blocking capacitor
C5	1µF	±20%	Supply voltage filter capacitor
C6	1µF	±20%	Supply voltage filter capacitor
C7	1µF	±20%	Supply voltage filter capacitor
C8	1µF	±20%	Supply voltage filter capacitor
C9*	3.3pF	±5%	Matching network capacitor for L1 band
	3.3pF	±5%	Matching network capacitor for L2/L3/L5 band
	3.3pF	±5%	Matching network capacitor for E6 band
	2.2pF	±5%	Matching network capacitor for S band
C10*	3.3pF	±5%	Matching network capacitor for L1 band
	3.3pF	±5%	Matching network capacitor for L2/L3/L5 band
	3.3pF	±5%	Matching network capacitor for E6 band
	2.2pF	±5%	Matching network capacitor for S band
C11	1µF	±20%	Supply voltage filter capacitor
C12	1µF	±20%	Supply voltage filter capacitor
C13*	33pF	±20%	Blocking capacitor
C14	1µF	±20%	Supply voltage filter capacitor
C15	10nF	±20%	Supply voltage filter capacitor
C16	10µF	±20%	Supply voltage filter capacitor
C17	1µF	±20%	Supply voltage filter capacitor
C18	1µF	±20%	Supply voltage filter capacitor
C19	1µF	±20%	Supply voltage filter capacitor
C20	1µF	±20%	Supply voltage filter capacitor
C21	1µF	±20%	Supply voltage filter capacitor
C22	1µF	±20%	Supply voltage filter capacitor
C23	1µF	±20%	Supply voltage filter capacitor
C24	1µF	±20%	Supply voltage filter capacitor
C25	1µF	±20%	Supply voltage filter capacitor
C26	1µF	±20%	Supply voltage filter capacitor
C27	1µF	±20%	Supply voltage filter capacitor
C28*	3.3pF	±5%	Matching network capacitor for L1 band
	3.3pF	±5%	Matching network capacitor for L2/L3/L5 band
	3.3pF	±5%	Matching network capacitor for E6 band
	2.2pF	±5%	Matching network capacitor for S band
L1*	7.5nH (Q≥40)	±2%	Matching network inductor for L1 band
	13nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	12nH (Q≥40)	±2%	Matching network inductor for E6 band
	2.9nH (Q≥40)	±2%	Matching network inductor for S band

Component	Nominal value	Tolerance	Notes
L2*	7.5nH (Q≥40)	±2%	Matching network inductor for L1 band
	13nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	12nH (Q≥40)	±2%	Matching network inductor for E6 band
	2.9nH (Q≥40)	±2%	Matching network inductor for S band
L3*	7.5nH (Q≥40)	±2%	Matching network inductor for L1 band
	13nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	12nH (Q≥40)	±2%	Matching network inductor for E6 band
	2.9nH (Q≥40)	±2%	Matching network inductor for S band
L4	120Ohm / 100MHz	±20%	Supply voltage filter inductor
L5*	7.5nH (Q≥40)	±2%	Matching network inductor for L1 band
	13nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	12nH (Q≥40)	±2%	Matching network inductor for L2/L3/L5 band
	2.9nH (Q≥40)	±2%	Matching network inductor for S band
R1	61.9kOhm	±1%	High precision resistor
R2*	200Ohm	±5%	Load resistor if analog differential output
	100Ohm	±5%	Load resistor if 2-bit ADC LVDS output
	–	–	DNP if 2-bit ADC CMOS output
R3*	200Ohm	±5%	Load resistor if analog differential output
	100Ohm	±5%	Load resistor if 2-bit ADC LVDS output
	–	–	DNP if 2-bit ADC CMOS output
R4*	200Ohm	±5%	Load resistor if analog differential output
	100Ohm	±5%	Load resistor if 2-bit ADC LVDS output
	–	–	DNP if 2-bit ADC CMOS output
R5*	200Ohm	±5%	Load resistor if analog differential output
	100Ohm	±5%	Load resistor if 2-bit ADC LVDS output
	–	–	DNP if 2-bit ADC CMOS output

Note: * – defined depending on PCB construction and purpose

4.3. PINS DESCRIPTION

Note: WLCSP balls that are not listed in Table 4.2 must be connected to the ground.

Table 4.2: NT1068.2 pin description

Pin	Ball	Name	Description
1	A12, B11, C10, D9	GND	Ground
2		GND	Ground
3	B12, C11, D10	RF2_GND	2nd channel RF ground
4		RF2_GND	2nd channel RF ground
5	C12	RF2_IN	2nd channel RF input (DC coupled)
6	B12, C11, D10	RF2_GND	2nd channel RF ground
7	E10	RF2_VCC	2nd channel “RF2” LDO output voltage
8	E11	MIX2_VCC	2nd channel “MIX2” LDO output voltage
9	F12	SPL_IN	Splitter input
10	F11	PLLA_GND	PLL “A” ground
11	F10	PLLA_VCC	PLL “A” LDO output voltage
12	G10	PLLB_VCC	PLL “B” LDO output voltage
13	G11	PLLB_GND	PLL “B” ground
14	J7	REF_CUR	External high-precision resistor connection
15	H11	MIX3_VCC	3rd channel “MIX3” LDO output voltage
16	H10	RF3_VCC	3rd channel “RF3” LDO output voltage
17	J10, K11, L12	RF3_GND	3rd channel RF ground
18	K12	RF3_IN	3rd channel RF input (DC coupled)
19	J10, K11, L12	RF3_GND	3rd channel RF ground
20		RF3_GND	3rd channel RF ground
21	J9, K10, L11, M12	GND	Ground
22		GND	Ground
23		GND	Ground
24		GND	Ground
25	K9, L10, M11	RF4_GND	4th channel RF ground
26		RF4_GND	4th channel RF ground
27	M10	RF4_IN	4th channel RF input (DC coupled)
28	K9, L10, M11	RF4_GND	4th channel RF ground
29	K8	RF4_VCC	4th channel “RF4” LDO output voltage
30	L8	MIX4_VCC	4th channel “MIX4” LDO output voltage
31	M8	RF4_GND	4th channel RF ground
32	K7	TEST	Test output; should be opened
33	L7	RO_GND	Reference oscillator ground
34	M7	REF_IN	Reference frequency (TCXO) input
35	K6	RO_VCC	“RO” LDO output voltage
36	L6, M6	IC_VCC	Supply voltage 1.8…3.3V
37	L5	IFA4_GND	4th channel IFA ground
38	K5	IFA4_VCC	4th channel “IFA4” LDO output voltage
39	L4	IFB4_GND	4th channel IF buffer & ADC ground
40	M4	IF4_OUTp/MAGN	4th channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement

Pin	Ball	Name	Description
41	M3	IF4_OUTn/SIGN	4th channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
42	L3	IFB4_VCC	4th channel "IFB4" LDO output supply
43	M2	IFB4_GND	4th channel IF buffer & ADC ground
44	J4, K3, L2, M1	GND	Ground
45		GND	Ground
46	L1	IFB3_GND	3rd channel IF buffer & ADC ground
47	K2	IFB3_VCC	3rd channel "IFB3" LDO output supply
48	K1	IF3_OUTn/SIGN	3rd channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
49	J1	IF3_OUTp/MAGN	3rd channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
50	J2	IFB3_GND	3rd channel IF buffer & ADC ground
51	H3	IFA3_VCC	3rd channel "IFA3" LDO output voltage
52	H2	IFA3_GND	3rd channel IFA ground
53	H1	CLK_GND	CLK management unit ground
54	G2	CLK_VCC	"CLK" LDO output voltage 1.7V...VCC (Reg12<D4–D0> dependent)
55	G1	CLK_OUT2	Clock frequency analog output – complement
56	F1	CLK_OUT1	Clock frequency analog output – true; CMOS output
57	F2	CLK_GND	CLK management unit ground
58	E1	CLK_GND	CLK management unit ground
59	E2	IFA2_GND	2nd channel IFA ground
60	E3	IFA2_VCC	2nd channel "IFA2" LDO output voltage
61	D2	IFB2_GND	2nd channel IF buffer & ADC ground
62	D1	IF2_OUTp/MAGN	2nd channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
63	C1	IF2_OUTn/SIGN	2nd channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
64	C2	IFB2_VCC	2nd channel "IFB2" LDO output voltage
65	B1	IFB2_GND	2rd channel IF buffer & ADC ground
66	A1, B2, C3, D4	GND	Ground
67		GND	Ground
68	A2	IFB1_GND	1st channel IF buffer & ADC ground
69	B3	IFB1_VCC	1st channel "IFB1" LDO output voltage
70	A3	IF1_OUTn/SIGN	1st channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
71	A4	IF1_OUTp/MAGN	1st channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement

Pin	Ball	Name	Description
72	B4	IFB1_GND	1st channel IF buffer & ADC ground
73	C5	IFA1_VCC	1st channel "IFA1" LDO output voltage
74	B5	IFA1_GND	1st channel IFA ground
75	B6	CSN	SPI chip select (active low)
76	A6	SCLK	SPI clock input
77	B7	MOSI	SPI data input
78	A7	MISO	SPI data output
79	C7	AOK	Cumulative status indicator: "1" valid "0" fail
80	A8	RF1_GND	1st channel RF ground
81	B8	MIX1_VCC	1st channel "MIX1" LDO output voltage
82	C8	RF1_VCC	1st channel "RF1" LDO output voltage
83	A11, B10, C9	RF1_GND	1st channel RF ground
84	A10	RF1_IN	1st channel RF input (DC coupled)
85	A11, B10, C9	RF1_GND	1st channel RF ground
86		RF1_GND	1st channel RF ground
87	A12, B11, C10, D9	GND	Ground
88		GND	Ground

Note: WLCSP balls that are not listed in Table 4.3 must be connected to the ground.

Table 4.3: NT1068.2 balls description

Ball	Pin	Name	Description
A3	70	IF1_OUTn/SIGN	1st channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
A4	71	IF1_OUTp/MAGN	1st channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
A6	76	SCLK	SPI clock input
A7	78	MISO	SPI data output
A10	84	RF1_IN	1st channel RF input (DC coupled)
B3	69	IFB1_VCC	1st channel "IFB1" LDO output voltage
B6	75	CSN	SPI chip select (active low)
B7	77	MOSI	SPI data input
B8	81	MIX1_VCC	1st channel "MIX1" LDO output voltage
C1	63	IF2_OUTn/SIGN	2nd channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
C2	64	IFB2_VCC	2nd channel "IFB2" LDO output voltage
C5	73	IFA1_VCC	1st channel "IFA1" LDO output voltage
C7	79	AOK	Cumulative status indicator: "1" valid "0" fail
C8	82	RF1_VCC	1st channel "RF1" LDO output voltage
C12	5	RF2_IN	2nd channel RF input (DC coupled)

Ball	Pin	Name	Description
D1	62	IF2_OUTp/MAGN	2nd channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
E3	60	IFA2_VCC	2nd channel “IFA2” LDO output voltage
E10	7	RF2_VCC	2nd channel “RF2” LDO output voltage
E11	8	MIX2_VCC	2nd channel “MIX2” LDO output voltage
F1	56	CLK_OUT1	Clock frequency analog output – true; CMOS output
F10	11	PLLA_VCC	PLL “A” LDO output voltage
F12	9	SPL_IN	Splitter input
G1	55	CLK_OUT2	Clock frequency analog output – complement
G2	54	CLK_VCC	“CLK” LDO output voltage 1.7V...VCC (Reg12<D4–D0> dependent)
G10	12	PLLB_VCC	PLL “B” LDO output voltage
H3	51	IFA3_VCC	3rd channel “IFA3” LDO output voltage
H10	16	RF3_VCC	3rd channel “RF3” LDO output voltage
H11	15	MIX3_VCC	3rd channel “MIX3” LDO output voltage
J1	49	IF3_OUTp/MAGN	3rd channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
J7	14	REF_CUR	External high-precision resistor connection
K1	48	IF3_OUTn/SIGN	3rd channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
K2	47	IFB3_VCC	3rd channel “IFB3” LDO output supply
K5	38	IFA4_VCC	4th channel “IFA4” LDO output voltage
K6	35	RO_VCC	“RO” LDO output voltage
K7	32	TEST	Test output; should be opened
K8	29	RF4_VCC	4th channel “RF4” LDO output voltage
K12	18	RF3_IN	3rd channel RF input (DC coupled)
L3	42	IFB4_VCC	4th channel “IFB4” LDO output supply
L6	36	IC_VCC	Supply voltage 1.8…3.3V
L8	30	MIX4_VCC	4th channel “MIX4” LDO output voltage
M3	41	IF4_OUTn/SIGN	4th channel analog output – complement; 2-bit ADC CMOS output data – SIGN; 2-bit ADC LVDS output – true
M4	40	IF4_OUTp/MAGN	4th channel analog output – true; 2-bit ADC CMOS output data – MAGN; 2-bit ADC LVDS output – complement
M6	36	IC_VCC	Supply voltage 1.8…3.3V
M7	34	REF_IN	Reference frequency (TCXO) input
M10	27	RF4_IN	4th channel RF input (DC coupled)

4.4. SERIAL INTERFACE DESCRIPTION

4.4.1. PROTOCOL DESCRIPTION

NT1068.2 can be configured with standard 4-wire SPI. In addition special pin "AOK" (cumulative status indicator) for unexpected system failure tracking is available.
User register map is split up into five parts according to functionality:

- System Info
- General settings and status
- CLK settings
- Channel settings and status (separate for each channel)
- PLL settings and status (separate for each PLL)

Available settings and statuses are listed in subsection 4.4.2.

4.4.1.1. GENERAL DESCRIPTION

Serial interface is used to read and change NT1068.2 data register information. It is intended for status monitoring, mode configuration and parameter adjustment.
Serial interface uses 4 pin for communication:

- CSN – serial interface enable chip select signal (low active)
- MISO – serial interface output data
- MOSI – serial interface input data
- SCLK – serial interface clock (low when idle)

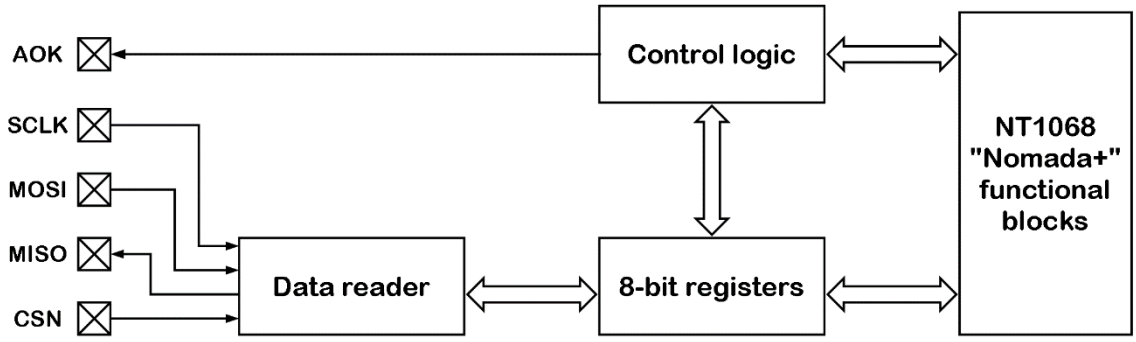


Figure 4.6: Serial interface structure

Standard information packet (command) consists of two bytes. The first byte is command/address, second – data byte. Data format is always a bit sequence from first MSB to last LSB. All data transfers are framed by CSN signal, which must be low for any data transfer. In "idle" state, when CSN is high, SCLK, MOSI and MISO pins are blocked and don't respond to external signals. At the beginning of any data transfer (falling CSN edge) SCLK must be low.

4.4.1.2. WRITING TO REGISTER

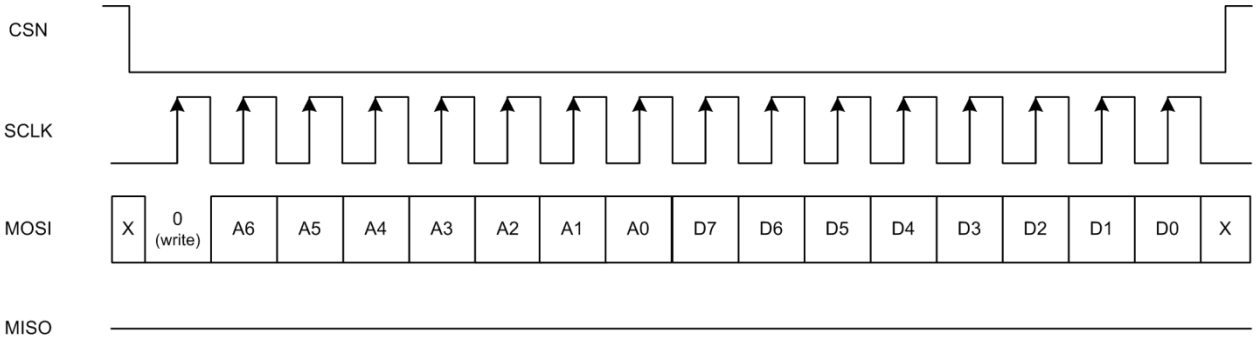


Figure 4.7: Individual register writing

Single write reading is shown on Figure 4.7. Communication is initialized by setting Chip Select (CSN) pin low. Bytes are transmitted MSB first. Data are clocked into the NT1068.2, through the MOSI pin, on the rising edges of SCLK. The first bit of a command/address byte is a read/write attribute: read operation is defined by logic "1" and write operation is defined by logic "0". Bits A6…A0 represent the address of the register to be read or written. Second byte (D7…D0 bits) is data written to the given address register. After the 16th rising SCLK edge and turn-off CSN hold time CSN goes high, disabling the interface.

4.4.1.3. READING FROM REGISTER

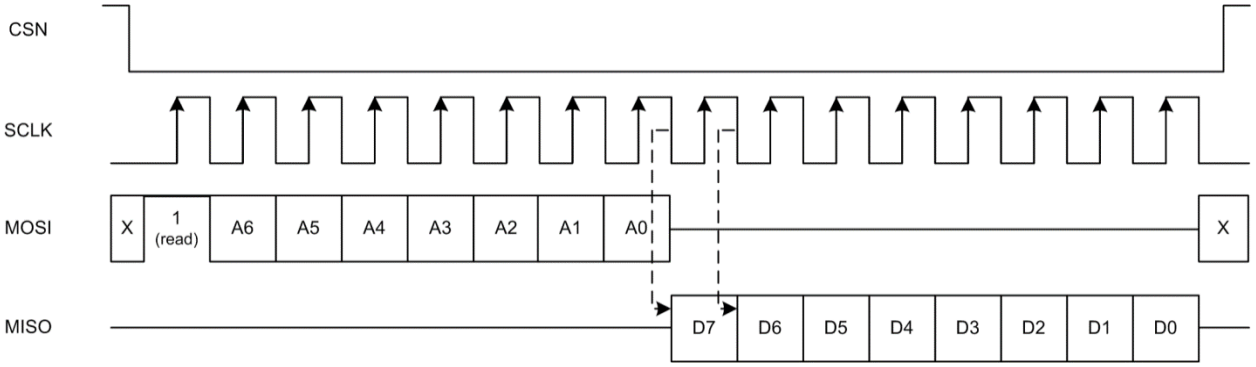


Figure 4.8: Single register reading

Single register reading is similar to writing. First byte is command byte. Read attribute is logic "1" and A6–A0 bits specify address of register to be read. Data are clocked out the NT1068.2, through the MISO pin, on the falling edges of SCLK. Output data should be clocked on rising SCLK edges of external SPI master. Bytes are transmitted MSB first. After sending data byte CSN goes high, disabling the interface.

4.4.1.4. BURST DATA TRANSFER

The NT1068.2 has a SPI burst-mode data transfer. Unlike single data transfer CSN is continue to be “low” after LSB of data byte. Next bit after LSB is a write/read attribute. CSN goes high to stop burst data transfer. Direction of data transfer can be changed an infinite number of times during burst data transfer. See examples below, please.

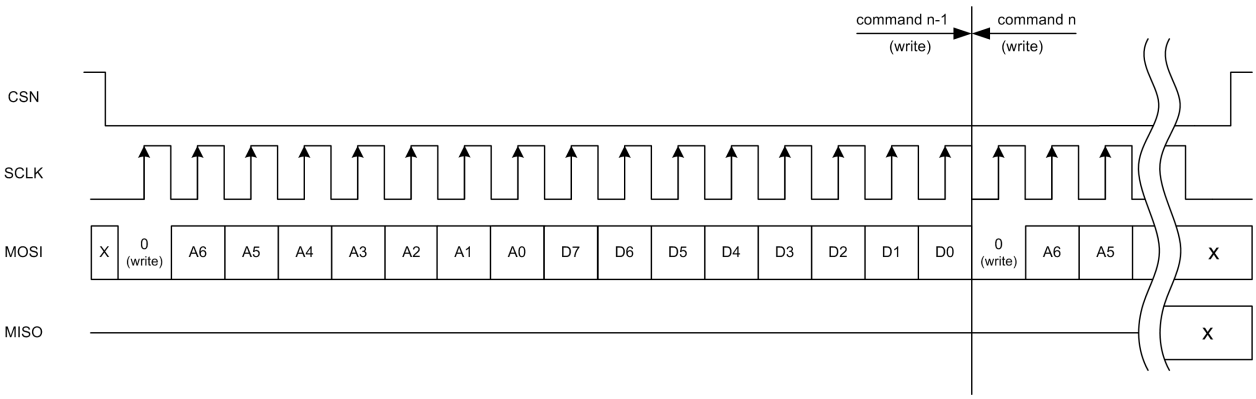


Figure 4.9: Burst data writing

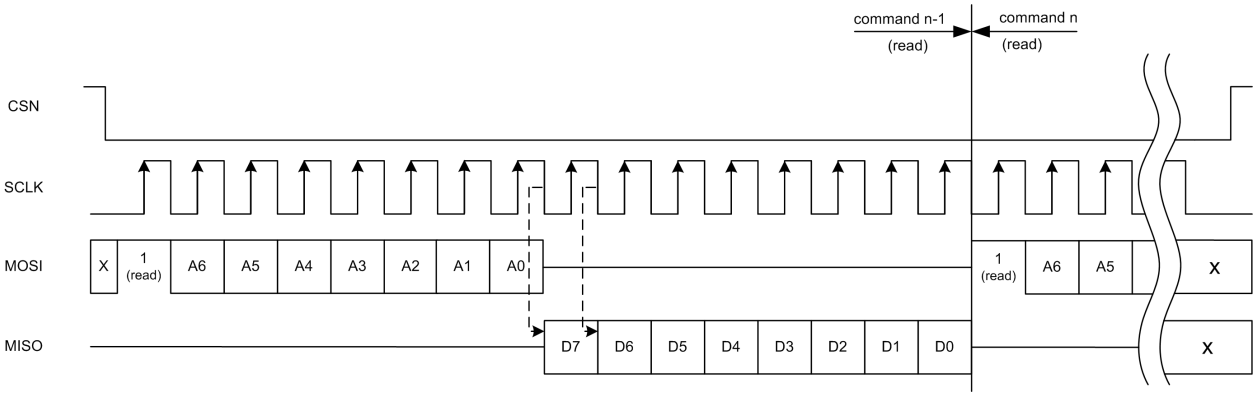


Figure 4.10: Burst data reading

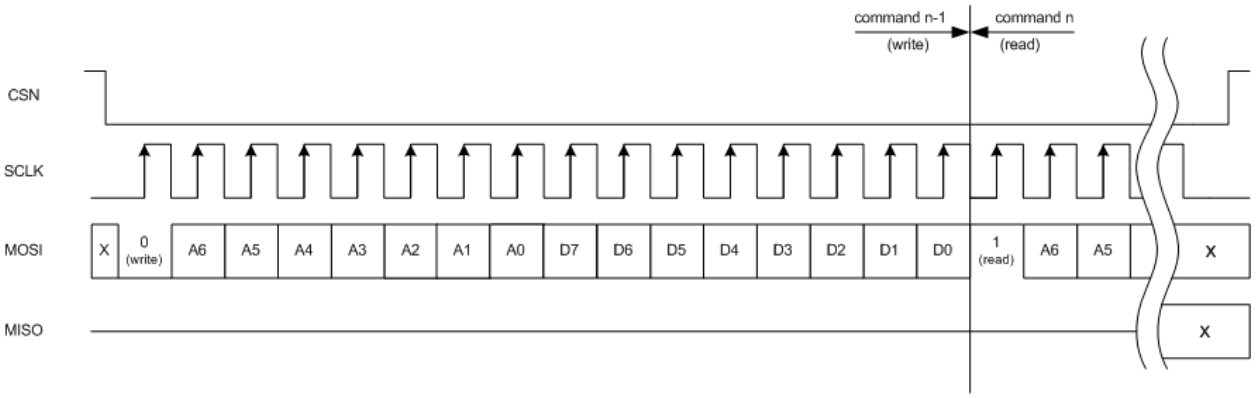


Figure 4.11: Burst data writing and reading

4.4.1.5. TIMING DIAGRAM

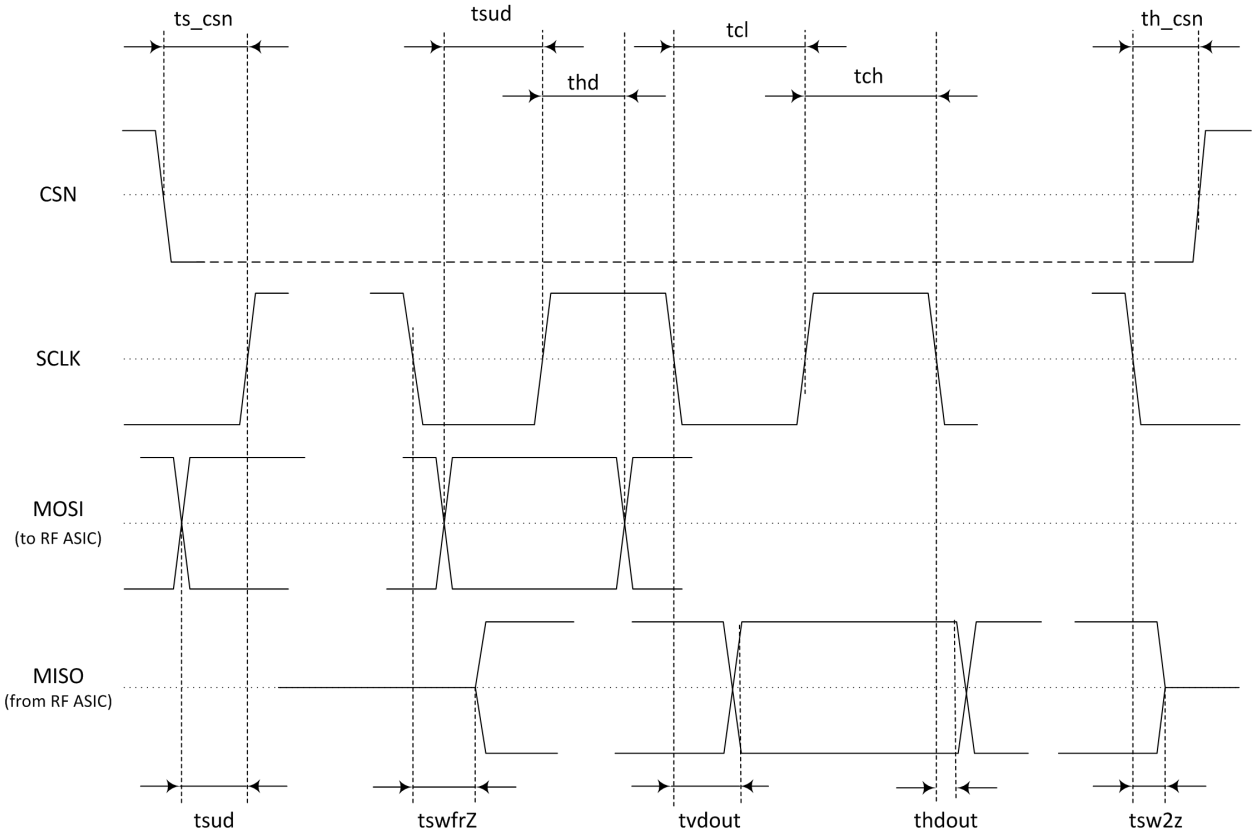


Figure 4.12: SPI timing diagram

Table 4.4: SPI timing

Parameter description	Symbol	Condition		Value min	Value typ.	Value max	Unit
SCLK frequency	fclk	V_{CC}=2.85–3.6V		–	–	40	MHz
		V_{CC}=1.71–2.85V		–	–	20	
SCLK high and low time	tch, tcl	1/fclk = (tch+tcl)	V_{CC}=2.85–3.6V	8	–	12	ns
			V_{CC}=1.71–2.85V	18	–	27	
Duty cycle	D	–		40	–	60	%
CSN setup time before SCLK	ts_csn	–		8	–	–	ns
CSN hold time	th_csn	–		4	–	–	ns
Data set up time	tsud	–		10	–	–	ns
Data hold time	thd	–		3	–	–	ns
Switch from Z-state time	tswfrZ	Load 20 pF		–	–	–	ns
Output data hold time	thdout	Load 20 pF		2.8	–	–	ns
Output data valid time	tvdout	Load 20 pF		–	–	10	ns
Switch to Z-state time	tsw2z	Load 20 pF		3	–	8	ns

4.4.2. PROGRAMMABLE REGISTERS

4.4.2.1. SYSTEM INFO

– ID number, release, version revision

Bit number	Name	Description	Default
Reg0, 0x00			
D7–D0	ID<12:5>	Technical information. Chip number. (0010000101100)bin = 1068dec	“00100001”
Reg1, 0x01			
D7–D3	ID<4:0>	Continue. Refer to Reg0<D7–D0>	“01100”
D2–D0	Release<2:0>	Technical information. Chip version. $(010)_{bin}$ =2dec	“010”

4.4.2.2. GENERAL SETTINGS AND STATUS

– Mode (standby, synthesizer only, active)
– Power economy mode
– Software reset
– Supply voltage (1.8V) source
– TCXO frequency setting (7 bits)
– LO source (PLL “A” for all channels; PLL “A” + PLL “B”)
– Channel# to be monitored for status (ch#1, ch#2, ch#3, ch#4)
– Temperature measurement mode (single, continuous)
– Temperature measurement system execute
– AOK indicator configuration
– General status (AOK, temperature, supply voltage level and failure indictors, reference frequency indicator)
– Selected channel status (RF AGC indicator, RF gain, IG gain)

Bit number	Name	Description	Default
Reg2, 0x02			
D7–D5	Version revision<2:0>	Version revision	“001”
D4	Service setting	Do not change	“0”
D3	SOFT_RESET	IC reset (is started and finished through SPI): “0” finish “1” start	“0”
D2	ECO_MD	Power economy mode: “0” disabled “1” enabled	“0”
D1–D0	Mode<1:0>	IC mode: “00” standby “01” PLL “A” only “10” PLL “A” only “11” active	“11”
		Note: As register bits are writable in any mode, exclude any configuration change in “standby” mode to return in last configured “active” mode.	

Bit number	Name	Description	Default
Reg3, 0x03			
D7–D1	TCXO_sel<6:0>	TCXO frequency setting: “0000000” 10 MHz “0000001” 24.84 MHz “0000010” 4.688 … 5.312 MHz … “0001000” 4.688 … 5.312 MHz … with step of 0.625MHz “1100000” 59.688 … 60.312 MHz “1100001” 60.313 … 60.937 MHz not guaranteed … with step of 0.625MHz “1111111” 79.063 … 79.687 MHz not guaranteed	“0000000”
D0	LO_Source	LO source: “0” PLL “A” for all channels “1” PLL “A” + PLL “B”	“1”
Reg4, 0x04			
D7–D2	Unused	Unused	“000000”
D1	Service status	May change its state	–
D0	Service setting	Is set to “1” at power up. Set to “0” when writing new configuration	“1”
Reg5, 0x05			
D7–D6	Unused	Unused	“00”
D5–D4	Ch_StNumSel<1:0>	Channel to be monitored for status: “00” Channel#1 “01” Channel#2 “10” Channel#3 “11” Channel#4	“00”
D3–D2	Unused	Unused	“00”
D1	TS_MD	Temperature measurement mode: “0” single “1” continuous	“0”
D0	TS_EXE	Temperature measurement system execute (duration is up to 17 ms and it automatically resets to “0” when finished): “0” finished “1” start	“0”
Reg6, 0x06			
D7	Unused	Unused	“0”
D6	SVFI_AOK	Supply voltage failure indicator as AOK’s component: “0” forbidden “1” permitted	“0”
D5	SAS_AOK	VCO subband autoselection system (SAS) status as AOK’s component: “0” forbidden “1” permitted	“0”
D4	Service setting	Is set to “1” at power up. Recommended value is “0”.	“1”
D3	PLL_LI_AOK	PLL “A” & “B” (if enabled) lock indicator as AOK’s components: “0” forbidden “1” permitted	“1”

Bit number	Name	Description	Default
D2	PLL_VCO_AOK	PLL "A" & "B" (if enabled) VCO input voltage comparator status as AOK's component: "0" forbidden "1" permitted	"1"
D1	RF_AGC_AOK	RF AGC indicators (all enabled channels) as AOK's components: "0" forbidden "1" permitted	"0"
D0	StdBy_AOK	IC standby mode as AOK's component (forces AOK to "0" in standby mode): "0" forbidden "1" permitted	"1"
Reg7, 0x07			
D7–D6	Unused	Unused	"000"
D5	FREF_FAULT	Reference frequency indicator: "0" ≥150kHz "1" <150kHz	–
D4	AOK	Cumulative status indicator: "0" fail "1" valid	–
D3	SVLI	Supply voltage level indicator: "0" $V_{CC} \geq 2.85V$ "1" $V_{CC} < 2.85V$	–
D2	SVFI	Supply voltage failure indicator: "0" fail (registers were reset to default states) "1" valid (should be manually set to detect next failure)	–
D1–D0	TS_code<9:8>	Temperature sensor indicator : "0000000000" not valid range … "0010111100" not valid range "0010111101" +125 °C … Temp = 206.67 - 0.4324*(TS_code<9:0>)$_{dec}$ "1000111011" –40 °C "1000111100" not valid range … "1111111111" not valid range **Note**: In continuous mode (TS_MD = "1") Reg7 <D1–D0> and Reg8 <D7–D0> must be read in series.	–
Reg8, 0x08			
D7–D0	TS_code<7:0>	Continue. Refer to Reg7<D1–D0> **Note**: In continuous mode (TS_MD = "1") Reg7 <D1–D0> and Reg8 <D7–D0> must be read in series.	–

Bit number	Name	Description	Default
Reg9, 0x09			
D7–D6	IFA_GainSt<1:0>	IFA fine power gain value status (refer to Reg5<D5–D4> for channel selection): "00000" –1.04 dB "00010" –0.79 dB "00100" –0.53 dB "00110" –0.28 dB "01000" –0.03 dB "01010" 0.23 dB "01100" 0.48 dB "01110" 0.73 dB "10000" 0.99 dB "10010" 1.24 dB "10100" 1.49 dB "10110" 1.74 dB "11000" 1.99 dB "11010" 2.25 dB "11100" 2.50 dB "11110" 2.75 dB "11111" 2.75 dB **Note:** Status of two least significant bits of IFA#_Gain<4:0> in automatic gain control mode.	–
D5–D4	RF_AGC_Down RF_AGC_Up	RF AGC indicator (refer to Reg5<D5–D4> for channel selection): "00" input signal power is within regulating range "01" input signal power is lower than threshold "10" input signal power is higher than regulating range "11" impossible state or RF AGC system is damaged	–
D3–D0	RF_GainSt<3:0>	RF power gain value status (refer to Reg5<D5–D4> for channel selection): L1 band / L2/L3/L5 band / S band "0000" 2.35 dB / 1.45 dB / 2.55 dB … with step of 0.95 dB "1111" 16.6 dB / 15.7 dB / 16.8 dB	–
Reg10, 0x0A			
D7–D5	IFA_GainSt<4:2>	Continue. Refer to Reg9 <D7–D6> **Note:** Status of three most significant bits of IFA#_Gain<4:0> in automatic gain control mode.	–
D4–D0	IFA_ManGC_St<4:0>	IFA coarse power gain value status (refer to Reg5<D5–D4> for channel selection): "00000" 9.65 dB "00010" 12.73 dB "00101" 18.88 dB "01000" 24.93 dB "01011" 30.89 dB "01110" 35.64 dB "10001" 41.79 dB "10100" 47.55 dB "10111" 52.19 dB "11010" 58.17 dB "11101" 64.20 dB "11111" 67.96 dB **Note:** Status of IFA#_ManGC<4:0> in automatic gain control mode.	–

4.4.2.3. CLK SETTINGS

- CLK frequency source (PLL “A”, PLL “B”, TCXO pass-through, disabled)
- CLK C-divider ratio (6 bits) // if PLL “A” or PLL “B” clock source
- TCXO frequency divider ratio (2 bits) // if TCXO pass-through mode
- CLK type (CMOS, differential, LVDS)
- CLK peak-to-peak voltage (230mV, 340mV, 450mV, 560mV) // if differential type
- CLK output DC level (2 bits) // if differential type
- CLK output logic-level high (1.8V, 2.4V, 2.7V, VCC) // if CMOS type
- CLK peak-to-peak voltage (350mV, 525mV, 700mV, 875mV) // if LVDS type

Bit number	Name	Description	Default
Reg11, 0x0B			
D7–D6	RO_CLK_R<1:0>	TCXO frequency divider ratio (if CLK_Source = “11”): “00” 1 “01” 2 “10” 4 “11” 8	“00”
D5	CDIV_R_EXT	Halving the step of F_{CLK} (refer to formula in section 7.11 for F_{CLK} calculation): “0” disabled “1” enabled	“0”
D4–D0	CDIV_R<4:0>	CLK C-divider ratio (refer to formula in section 7.11 for F_{CLK} calculation): “01000” 8 … with step of 1 “11111” 31	“01111”
Reg12, 0x0C			
D7	CLK_LVDS	CLK LVDS type: “0” disabled “1” enabled (recommended if IFA#_ADC_LVDS = “1”)	“0”
D6–D5	CLK_Source<1:0>	CLK frequency source: “00” PLL “A” “01” PLL “B” “10” disabled (allowed if IFA#_OT= “0” or IFA#_OT= “1”& IFA#_ADC_Clk<1:0>=“0X”) “11” TCXO pass-through	“00”
D4	CLK_TP	CLK type if CLK_LVDS = “0”: “0” CMOS “1” differential	“1”
D3–D2	CLK_CC<1:0>	CLK peak-to-peak voltage if CLK_TP = “1” (with R_{load} / without R_{load}): “00” 0.23 / 0.46 V “01” 0.34 / 0.69 V “10” 0.45 / 0.92 V “11” 0.56 / 1.13 V CLK peak-to-peak voltage at R_{load} if CLK_LVDS=“1” (ECO=0 / ECO=1): 350 mV / 200 mV 525 mV / 300 mV 700 mV / 400 mV 875 mV / 500 mV	“10”

Bit number	Name	Description	Default
D1–D0	CLK_OL<1:0>	CLK output logic-level high if CLK_TP = "0": $V_{CC} \geq 2.85V$: / $V_{CC} < 2.85V$: "00" 1.8 V / 1.8 V "01" 2.4 V / 1.8 V "10" 2.7 V / 1.8 V "11" external (VCC) / external (VCC) CLK output DC level if CLK_TP = "1": $V_{CC} \geq 2.85V$: / $V_{CC} < 2.85V$: "00" $(1.8 – 0.55 \times V_{CLK})$ V / $(1.8 – 0.55 \times V_{CLK})$ V "01" $(2.4 – 0.55 \times V_{CLK})$ V / $(1.8 – 0.55 \times V_{CLK})$ V "10" $(2.7 – 0.55 \times V_{CLK})$ V / $(1.8 – 0.55 \times V_{CLK})$ V "11" $(VCC – 0.55 \times V_{CLK})$ V / $(VCC – 0.55 \times V_{CLK})$ V	"00"

4.4.2.4. CHANNEL SETTINGS

- Channel enable
- Splitter enable
- Channel mode (lower sideband, upper sideband)
- IF passband (7 bits, 11 – 33 MHz)
- Output data interface (analog differential output, 2-bit ADC output)
- IFA output DC level (2 bits)
- RF GC mode (manual, auto)
- IFA GC mode (manual, auto)
- RF AGC thresholds (4bits for upper threshold, 4 bits for lower threshold)
- IF AGC threshold (200mV, 400mV)
- RF gain in manual mode (4 bits)
- IF gain in manual mode (10 bits)
- IF AGC digital detector threshold
- Channel output load 200Ohm external resistor (yes, no)
- ADC output type (CMOS, LVDS)
- ADC output logic-level high (1.8V, 2.4V, 2.7V, VCC) // if CMOS output type
- ADC output current (1.8mA, 2.6mA, 3.5mA, 4.4mA) // if LVDS output type
- ADC type (asynchronous, clocked by rising edge, clocked by falling edge)

Bit number	Name	Description	Default
Reg13, 0x0D for Channel#1 / Reg20, 0x14 for Channel#2 / Reg27, 0x1B for Channel#3 / Reg34, 0x22 for Channel#4			
D7–D3	Unused	Unused	"00000"
D2	SPL_Ch#	Splitter input for Channel#: "0" disabled "1" enabled	"0"
D1	Ch#_LSB	Channel# GNSS: "0" upper sideband "1" lower sideband	Ch#1&4 "1" Ch#2&3 "0"
D0	Ch#_EN	Channel# enable: "0" disabled "1" enabled	"1"

Bit number	Name	Description	Default
Reg14, 0x0E for Channel#1 / Reg21, 0x15 for Channel#2 / Reg28, 0x1C for Channel#3 / Reg35, 0x23 for Channel#4			
D7	Unused	Unused	"0"
D6–D0	LPF_code#<6:0>	IF passband: "0000000" unused … … "0000110" unused "0000111" 11.1 MHz … … "0001100" 12.1 MHz … … "0010010" 13.4 MHz … … "0010101" 14.0 MHz … … "0011110" 15.9 MHz … … "0100000" 16.3 MHz (default for Channel#4) … … "0100100" 17.1 MHz … … "0100111" 17.7 MHz … … "0101101" 19.0 MHz … … "0110000" 19.6 MHz … … "0110110" 20.8 MHz … … "0111001" 21.4 MHz … … "0111100" 22.0 MHz … … "0111110" 22.5 MHz (default for Channel#3) … … "1000011" 23.5 MHz … … "1001000" 24.5 MHz (default for Channel#2) … … "1010010" 26.4 MHz (default for Channel#1) "1010011" 26.6 MHz "1010100" 26.7 MHz … … "1111111" 33.0 MHz	Ch#1 "1010010" Ch#2 "1001000' Ch#3 "0111110" Ch#4 "0100000"
Reg15, 0x0F for Channel#1 / Reg22, 0x16 for Channel#2 / Reg29, 0x1D for Channel#3 / Reg36, 0x24 for Channel#4			
D7	Unused	Unused	"0"
D6	IFA#_AmpLvl	IF AGC threshold (w.r.t. sinewave signal): "0" 200 mV "1" 400 mV	"0"
D5	IFA#_ResLoad	Channel output load 200 Ohm external resistor: "0" not mounted "1" mounted	"1"
D4	RF#_AGC_MD	RF GC mode: "0" manual gain control (refer to RF#_Gain<3:0> to set gain) "1" automatic gain control (refer to RF#_AGC_UB<2:0> and RF#_AGC_LB<2:0> to set thresholds)	"0"

Bit number	Name	Description	Default
D3	IFA#_AGC_MD	IFA GC mode: "0" manual gain adjustment (refer to IFA#_ManGC<4:0> and IFA#_Gain<4:0> to set gain) "1" automatic gain control	"1"
D2–D1	IFA#_OP<1:0>	IFA output DC level (if IFA#_OT = "0"): $V_{CC} \geq 2.85V$: / $V_{CC} < 2.85V$: "00" 1.75 V / 1.2 V "01" 1.95 V / 1.2 V "10" 2.1 V / 1.2 V "11" 2.2 V / $0.4 \times V_{CC}+0.45$	"01"
D0	IFA#_OT	Output data interface: "0" analog differential output "1" 2-bit ADC output	"0"
Reg16, 0x10 for Channel#1 / Reg23, 0x17 for Channel#2 / Reg30, 0x1E for Channel#3 / Reg37, 0x25 for Channel#4			
D7–D4	RF#_AGC_UB<3:0>	RF AGC upper threshold (w.r.t. sinewave signal input power): "0000" –45.2 dBm "0001" –43.9 dBm "0010" –42.8 dBm "0011" –41.9 dBm "0100" –41.1 dBm "0101" –40.5 dBm "0110" –39.8 dBm "0111" –39.2 dBm "1000" –38.8 dBm "1001" –38.3 dBm "1010" –37.9 dBm "1011" –37.5 dBm "1100" –37.1 dBm "1101" –36.7 dBm "1110" –36.3 dBm "1111" –36.0 dBm	"0011"
D3–D0	RF#_AGC_LB<3:0>	RF AGC lower threshold (w.r.t. sinewave signal input power): "0000" –48.4 dBm "0001" –47 dBm "0010" –46 dBm "0011" –45.2 dBm "0100" –44.5 dBm "0101" –43.9 dBm "0110" –43.3 dBm "0111" –42.8 dBm "1000" –42.3 dBm "1001" –42 dBm "1010" –41.5 dBm "1011" –41.1 dBm "1100" –40.8 dBm "1101" –40.4 dBm "1110" –40.1 dBm "1111" –39.8 dBm	"0100"
Reg17, 0x11 for Channel#1/ Reg24, 0x18 for Channel#2/ Reg31, 0x1F for Channel#3/ Reg38, 0x26 for Channel#4			
D7–D4	RF#_Gain<3:0>	RF power gain in manual mode (if RF#_AGC_MD = "0"): L1 band / L2/L3/L5 band / S band "0000" 2.35 dB / 1.45 dB / 2.55 dB … with step of 0.95 dB "1111" 16.6 dB / 15.7 dB / 16.8 dB	"1111"

Bit number	Name	Description	Default
D3–D2	Unused	Unused	“00”
D1–D0	IFA#_ManGC<4:3>	IFA coarse power gain value in manual mode (IFA#_AGC_MD = "0"): “00000” 9.65 dB “00010” 12.73 dB “00101” 18.88 dB “01000” 24.93 dB “01011” 30.89 dB “01110” 35.64 dB “10001” 41.79 dB “10100” 47.55 dB “10111” 52.19 dB “11010” 58.17 dB “11101” 64.20 dB “11111” 67.96 dB	“01”
Reg18, 0x12 for Channel#1 / Reg25, 0x19 for Channel#2 / Reg32, 0x20 Channel#3 / Reg39, 0x27 for Channel#4			
D7–D5	IFA#_ManGC<2:0>	Continue. Refer to Reg17<D1–D0>	“111”
D4–D0	IFA#_Gain<4:0>	IFA fine power gain value in manual mode (if IFA#_AGC_MD = “0”): “00000” –1.04 dB “00010” –0.79 dB “00100” –0.53 dB “00110” –0.28 dB “01000” –0.03 dB “01010” 0.23 dB “01100” 0.48 dB “01110” 0.73 dB “10000” 0.99 dB “10010” 1.24 dB “10100” 1.49 dB “10110” 1.74 dB “11000” 1.99 dB “11010” 2.25 dB “11100” 2.50 dB “11110” 2.75 dB “11111” 2.75 dB IF AGC digital detector threshold w.r.t. sinewave signal (if IFA#_AGC_MD = “1”) & (IFA#_OT = “1”): “00000” 0.2% … … “00100” 15.1% … … “01001” 27.8% “01010” 30.3% “01011” 32.4% “01100” 34.5% “01111” 41.0% “10000” 43.2% … … “10011” 49.8% … … “11000” 60.8% “11001” not valid range … not valid range “11111” not valid range	“01010”
Reg19, 0x13 for Channel#1 / Reg26, 0x1A for Channel#2 / Reg33, 0x21 for Channel#3 / Reg40, 0x28 for Channel#4			
D7–D5	Unused	Unused	“000”
D4	IFA#_ADC_LVDS	ADC output type (if IFA#_OT = “1”): “0” CMOS “1” LVDS	“0”
D3–D2	IFA#_ADC_Clk<1:0>	ADC clocking type (if IFA#_OT = “1”): “0X” asynchronous (for IFA#_ADC_LVDS =“0” only) “10” by rising edge “11” by falling edge	“10”
D1–D0	IFA#_ADC_OL<1:0>	ADC output logic-level high (if IFA#_OT = “1” and IFA#_ADC_LVDS = “0”): $V_{CC} \geq 2.85V$: $V_{CC} < 2.85V$: “00” 1.8 V 1.8 V “01” 2.4 V 1.8 V “10” 2.7 V 1.8 V “11” ext. (V_{CC}) ext. (V_{CC}) ADC output current if IFA#_OT = “1” and IFA#_ADC_LVDS= “1” (ECO=0 / ECO=1): 1.8 mA / 1.0mA 2.6 mA / 1.5mA 3.5 mA / 2.0mA 4.4 mA / 2.5mA	“10”

4.4.2.5. PLL SETTINGS AND STATUS

- PLL enable
- Frequency band
- N-divider ratio (10 bits)
- R-divider ratio (4 bits)
- PLL tuning system execute
- Status (VCO input voltage comparator, lock indicator)

Bit number	Name	Description	Default
Reg41, 0x29			
D7–D3	Unused	Unused	“00000”
D2–D1	PLL_A_Band<1:0>	PLL “A” frequency band: LO_source=“0” LO_source=“1” “00” L2/L3/L5 L2/L3/L5 “01” L1 L1 “10” S L2/L3/L5 for ch#2 (Galileo) “11” unused S for ch#1 + L2 for ch#2 (NavIC) **Note:** If LO_source=“1” and PLL_A_Band<1:0>=“10”, then PLL_B_Band<1:0> = “10” must be selected. Other states of PLL_B_Band<1:0> are forbidden.	“01”
D0	PLL_A_EN	PLL “A” enable: “0” disabled “1” enabled	“1”
Reg42, 0x2A			
D7–D0	NDIV_R_A<8:1>	PLL “A” N-divider ratio (refer to formula in section 7.2 for F_{LO} calculation): “000001000” 8 … with step of 1 “111111111” 511	“01001111”
Reg43, 0x2B			
D7	NDIV_R_A<0>	Continue. Refer to Reg42<D7–D0>.	“1”
D6–D3	RDIV_R_A<3:0>	PLL “A” R-divider ratio (refer to formula in section 7.3 for F_{LO} calculation): “0001” 1 … with step of 1 “1111” 15	“0001”
D2	NDIV_R_A_EXT	Halving the step of PLL “A” F_{LO} (refer to formula in section 7.3 for F_{LO} calculation): “0” disabled “1” enabled	“0”
D1	Unused	Unused	“0”
D0	PLL_EXE_A	PLL “A” tuning system execute: “0” finished ”1” start (reset to “0” automatically when finished)	“0”
Reg44, 0x2C			
D7–D3	Unused	Unused	“00000”
D2–D1	VcoA_CVL VcoA_CVH	PLL “A” VCO input voltage indication: “00” valid “01” upper threshold exceeded (oscillation frequency is too low) “10” lower threshold exceeded (oscillation frequency is too high) “11” unused	–
D0	PLL_LI_A	PLL “A” lock indicator: “0” not locked “1” locked	–

Bit number	Name	Description	Default
Reg45, 0x2D			
D7–D3	Unused	Unused	"00000"
D2–D1	PLL_B_Band<1:0>	PLL "B" frequency band (if LO_source="1"): "00" L2/L3/L5 "01" L1 "10" L1 for ch#3 + L3&L5 for ch#1&4 (Galileo) "11" L1 for ch#3 + L3/L5 for ch#4 (NavIC) **Note:** If LO_source="1" and PLL_B_Band<1:0>="10", then PLL_A_Band<1:0> = "10" must be selected. Other states of PLL_A_Band<1:0> are forbidden.	"00"
D0	PLL_B_EN	PLL "B" enable: "0" disabled "1" enabled	"1"
Reg46, 0x2E			
D7–D0	NDIV_R_B<8:1>	PLL "B" N-divider ratio (refer to formula in section 7.2 for F_{LO} calculation): "000001000" 8 … with step of 1 "111111111" 511	"01111011"
Reg47, 0x2F			
D7	NDIV_R_B<0>	Continue. Refer to Reg46<D7–D0>.	"1"
D6–D3	RDIV_R_B<3:0>	PLL "B" R-divider ratio (refer to formula in section 7.2 for F_{LO} calculation): "0001" 1 … with step of 1 "1111" 15	"0010"
D2	NDIV_R_B_EXT	Halving the step of PLL "B" F_{LO} (refer to formula in section 7.3 for F_{LO} calculation): "0" disabled "1" enabled	"0"
D1	Unused	Unused	"0"
D0	PLL_EXE_B	PLL "B" tuning system execute: "0" finished "1" start (reset to "0" automatically when finished)	"0"
Reg48, 0x30			
D7–D3	Unused	Unused	"00000"
D2–D1	VcoB_CVL VcoB_CVH	PLL "B" VCO input voltage indication: "00" valid "01" upper threshold exceeded (oscillation frequency is too low) "10" lower threshold exceeded (oscillation frequency is too high) "11" unused	–
D0	PLL_LI_B	PLL "B" lock indicator: "0" not locked "1" locked	–

5. OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage –0.3…+ 3.6 V
Maximum input signal level +10 dBm
Input pin voltage –0.3… +3.6V
Storage temperature –55…+125 °C
Soldering temperature +260 °C
Electrostatic discharge rating (JESD78D Class II, Level A):

- HBM (pins 5, 18, 27, 84) 0.5 kV
- HBM (pins 14, 34, 40, 41, 48, 49, 55, 56, 62, 63, 70, 71, 75–79) 1 kV
- HBM (except pins 5, 14, 18, 27, 34, 40, 41, 48, 49, 55, 56, 62, 63, 70, 71, 75–79, 84) 2 kV

5.1. DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.71 V to 3.6 V, T_A= –40…+85°C. Typical values are at V_{cc} = 3.0 V, T_A=+25°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Supply voltage	V_{CC}	–		1.71	–	3.6	V
Current consumption	I_{CC_RF}	Note 1	@ RF inputs	–	110.5	–	mA
	I_{CC_SPL}		@ splitter input	–	116.5	–	mA
Leakage current		Shutdown mode		–	0.5	–	uA
Input logic-level low	V_{IL}	–		0	–	0.3	V
Input logic-level high	V_{IH}	–		V_{cc} – 0.3	–	V_{cc}	V
Output logic-level low	V_{OL}	I_{LOAD} = 100uA		0	–	0.3	V
Output logic-level high	V_{OH}	I_{LOAD} = 100uA		V_{cc} – 0.3	–	V_{cc}	V
ADC CMOS output logic-level high	V_{OH_ADC}	V_{CC}=1.71–2.85V, I_{LOAD} = 0mA/2mA	Preset 1–3	–	1.8/1.7	–	V
			Preset 4	–	V_{CC} / V_{CC} – 0.2	–	
		V_{CC}=2.85–3.6V , I_{LOAD} = 0mA/2mA	Preset 1	–	1.8/1.7	–	
			Preset 2	–	2.4/2.3	–	
			Preset 3	–	2.7/2.6	–	
			Preset 4	–	V_{CC} / V_{CC} – 0.2	–	
ADC CMOS output logic-level low	V_{OL_ADC}	I_{LOAD} =2mA		0	–	0.4	V
ADC LVDS output DC level	V_{DC_LVDS}	–		–	1.25	–	V
ADC LVDS output current	I_{LVDS}	R_{LOAD} = 100Ohm	Preset 1	–	1.8	–	mA
			Preset 2	–	2.6	–	
			Preset 3	–	3.5	–	
			Preset 4	–	4.4	–	
IFA analog output DC level	V_{DC_IFA}	V_{CC}=1.71–2.85V	Preset 1–3	–	1.2	–	V
			Preset 4	–	0.4×V_{CC}+0.45	–	
		V_{CC}=2.85–3.6V	Preset 1	–	1.75	–	
			Preset 2	–	1.95	–	
			Preset 3	–	2.1	–	
			Preset 4	–	2.2	–	
Differential clock output DC level	V_{DC_CLK}	V_{CC}=1.71–2.85V, V_{CLK}=0.45V	Preset 1–3	–	1.55	–	V
			Preset 4	–	V_{CC}–0.25	–	
		V_{CC}=2.85–3.6V, V_{CLK}=0.45V	Preset 1	–	1.55	–	
			Preset 2	–	2.15	–	
			Preset 3	–	2.45	–	
			Preset 4	–	V_{CC}–0.25	–	
Die temperature measurement range	T_j	–		–40	25	+125	°C
Die temperature measurement accuracy	ΔT_j	–		–	±5	–	°C

Note 1: 4 channels (2 L1 band @ PLL "A" + 2 L2/L3/L5 band @ PLL "B"), analog differential output, IF AGC threshold = 200mV, Vcc=1.8V

5.2. AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.71 V to 3.6 V, T_A=–40…+85°C. Typical values are at V_{cc} = 3.0 V, T_A =+25°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Overall							
Input frequency range	F_{IN}	L1 band		1530	–	1610	MHz
		L2/L3/L5 band		1150	–	1300	
		S band		2460	–	2530	
Reference frequency (TCXO) range	F_{REF}	–		5	10/24.84	60	MHz
Noise figure	NF_{RF_IN}	Referred to RF inputs, Note 2	L1 band	–	4.6	–	dB
			L2/L3/L5 band	–	5.7	–	
			S band	–	7.9	–	
		Referred to splitter input, Note 3	L1 band	–	19.0	–	
			L2/L3/L5 band	–	17.6	–	
			S band	–	20.5	–	
1 dB compression point	$P_{1dB\_RF\_IN}$	Referred to RF inputs, Note 4	L1 band	–	-25.0	–	dBm
			L2/L3/L5 band	–	-24.0	–	
			S band	–	-23.0	–	
		Referred to RF inputs, Note 5	L1 band	–	-39.0	–	
			L2/L3/L5 band	–	-35.0	–	
			S band	–	-35.0	–	
		Referred to splitter input, Note 6	L1 band	–	-21.0	–	
			L2/L3/L5 band	–	-21.0	–	
			S band	–	-23.0	–	
Total power gain	G_{MAX}	Referred to RF inputs	L1 band	–	87.3	–	dB
			L2/L3/L5 band	–	86.4	–	
			S band	–	87.5	–	
		Referred to splitter input	L1 band	–	71.3	–	
			L2/L3/L5 band	–	70.4	–	
			S band	–	71.5	–	
Channel isolation	Ch_{ISO}	–		–	35	–	dB
RF AGC range	ΔG_{RF}	Referred to RF inputs		–	14.25	–	dB
IF AGC range	ΔG_{IF}	–		–	62.1	–	dB
Group time delay ripple*	ΔT_{GD}	F_{IF} = 3 – 9MHz, F_{cut_LPF} = 18 MHz		–	<25	–	ns
		F_{IF} = 6 – 18MHz, F_{cut_LPF} = 25 MHz		–	<17	–	
Splitter&MIX							
Splitter&Mixer power gain	G_{SPL}	R_{IN_RF} = 50 Ohm, R_{OUT_RF} = 2kOhm	L1 band	–	0.6	–	dB
			L2/L3/L5 band	–	–0.3	–	
			S band	–	0.8	–	
Image rejection	IR	–		–	35	–	dB
Splitter input VSWR	$VSWR_{SPL\_IN}$	Without matching circuit @ 50 Ohm	L1 band	–	2.7	–	–
			L2/L3/L5 band	–	2.6	–	
			S band	–	2.0	–	
Preamp&MIX							
RF (Preamp&Mixer) max power gain	G_{MAX_RF}	R_{IN_RF} = 50Ohm, R_{OUT_RF} =2kOhm	L1 band	–	16.6	–	dB
			L2/L3/L5 band	–	15.7	–	
			S band	–	16.8	–	
RF (Preamp&Mixer) min power gain	G_{MIN_RF}	R_{IN_RF} = 50Ohm, R_{OUT_RF} =2kOhm	L1 band	–	2.35	–	dB
			L2/L3/L5 band	–	1.45	–	
			S band	–	2.55	–	
Preamp gain step	G_{STEP_MIX}	Referred to RF inputs		–	0.95	–	dB

Parameter	Symbol	Condition		Value			Unit
				min	typ.	max	
Image rejection	IR	–		–	35	–	dB
Preamplifier input VSWR	$VSWR_{RF\_IN}$	With matching circuit @ 50 Ohm	L1 band	–	1.5	–	–
			L2/L3/L5 band	–	2.0	–	
			S band	–	1.5	–	
LPF&IFA							
Output frequency range	F_{IF}	Tunable		3	–	33	MHz
LPF 3dB cut-off frequency	F_{cut_LPF}	Tunable, relative to 8 MHz		11	–	33	MHz
IF (LPF&IFA) max power gain	G_{MAX_IF}	R_{IN_IF}=2kOhm, R_{OUT_IF}=200 Ohm		–	70.7	–	dB
IF (LPF&IFA) min power gain	G_{MIN_IF}	R_{IN_IF}=2kOhm, R_{OUT_IF}=200 Ohm		–	8.6	–	dB
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	V_m	Note 7	Preset 1	–	200/470	–	mVp-p
			Preset 2	–	400/980	–	
Output resistance	R_{out}	Analog differential output		–	200	–	Ohm
ADC							
Resolution	R_{ADC}	–		–	2	–	bit
ADC CMOS output logic-level high	V_{OH_ADC}	V_{CC}=1.71–2.85V, I_{LOAD} = 0mA/2mA	Preset 1–3	–	1.8/1.7	–	V
			Preset 4	–	V_{CC}/V_{CC}–0.2	–	
		V_{CC}=2.85–3.6V, I_{LOAD} = 0mA/2mA	Preset 1	–	1.8/1.7	–	
			Preset 2	–	2.4/2.3	–	
			Preset 3	–	2.7/2.6	–	
			Preset 4	–	V_{cc} /V_{cc} – 0.2	–	
ADC LVDS output current	I_{LVDS}	R_{LOAD} = 100Ohm	Preset 1	–	1.8	–	mA
			Preset 2	–	2.6	–	
			Preset 3	–	3.5	–	
			Preset 4	–	4.4	–	
Synthesizer							
Reference frequency (TCXO)	F_{REF}	–		5	10/24.84	60	MHz
Reference input level	REF_{IN}	Sine or triangle wave	V_{CC}=1.71–2.85V	0.6	1	1.6	Vp-p
			V_{CC}=2.85–3.6V	0.6	1	2	
LO frequency range	F_{LO}	L1 band		1450	–	1620	MHz
		L2, L3, L5 band		1140	–	1300	
		S band		2280	–	2600	
VCO frequency range	F_{VCO}	VCO #1		2900	–	3240	MHz
		VCO #2		2280	–	2600	
VCO to PFD frequency integer-valued division ratio	N	–		16	–	1023	–
VCO to CLK frequency integer-valued division ratio	C	Multiple of 2		32	–	126	–
Reference frequency (TCXO) to PFD frequency integer-valued division ratio	R	–		1	–	15	–
Reference frequency (TCXO) to CLK frequency integer-valued division ratio	T	–		1	–	8	–
LO phase noise	PN_{LO}	F_{PFD}= 10 MHz, F_{LO} = 1590 MHz	@100 kHz	–	-95.5	–	dBc/Hz
			@1 MHz	–	-120.7	–	
		F_{PFD}= 5 MHz, F_{LO} = 1235 MHz	@100 kHz	–	-97.8	–	
			@1 MHz	–	-124.2	–	
		F_{PFD}= 10 MHz, F_{LO} = 2480 MHz	@100 kHz	–	-90.8	–	
			@1 MHz	–	-117.8	–	
LO RMS jitter	J_{RMS}	Integrated BW = 25 MHz		–	3.5	–	ps

Parameter	Symbol	Condition		Value			Unit
				min	typ.	max	
Clock frequency range (tunable)	F_{CLK}	F_{LO} = 1589.76 MHz		25.641	–	99.36	MHz
		F_{LO} = 1233.72 MHz		19.899	–	77.107	
		F_{LO} = 1590 MHz		25.645	–	99.375	
		F_{LO} = 1240 MHz or F_{LO} = 2480 MHz		20	–	77.5	
		TCXO pass-through mode		5	–	60	
Peak-to-peak voltage at the differential clock outputs	V_{CLK}	Diff clock mode R_{LOAD} = 200/-- Ohm, F_{CLK} < 50 MHz, C_{load} < 10pF	Preset 1	–	230/460	–	mVpp
			Preset 2	–	340/690	–	
			Preset 3	–	450/920	–	
			Preset 4	–	560/1130	–	
		LVDS mode R_{LOAD} = 100Ohm	Preset 1	–	350	–	mVpp
			Preset 2	–	525	–	
			Preset 3	–	700	–	
			Preset 4	–	875	–	
Output logic-level high at CMOS clock output	V_{OH_CLK}	V_{CC}=1.71–2.85V, F_{CLK} < 50MHz, C_{load} < 5pF	Preset 1–3	–	1.8	–	V
			Preset 4	–	V_{CC}	–	
		V_{CC}=2.85–3.6V, F_{CLK} < 50MHz, C_{load} < 5pF	Preset 1	–	1.8	–	
			Preset 2	–	2.4	–	
			Preset 3	–	2.7	–	
			Preset 4	–	V_{CC}	–	
Output logic-level low at CMOS clock output	V_{OL_CLK}	–		0	–	0.2	V
PFD frequency range	F_{CMP}	–		2	10/24.84	60	MHz

Notes:
* Guaranteed by simulation
Note 2: RFAGC = max gain, IFAGC gain > 30 dB
Note 3: IFAGC gain > 30 dB
Note 4: RFAGC = min gain, IFAGC = min gain
Note 5: RFAGC = max gain, IFAGC = min gain
Note 6: IFAGC = min gain
Note 7: RMS value measured. $V_{p\text{-}p\ sin} = V_{RMS}*2\sqrt{2}$; $V_{p\text{-}p\ noise} = V_{RMS}*6.6$

6. TYPICAL CHARACTERISTICS

Will be added.

6.1. TYPICAL S11 PARAMETERS

Will be added.

6.2. IBIS MODEL

Will be added.

7. APPLICATION NOTES

Some tricks or not obvious actions as well as configuration examples are described in this section.

7.1. REFERENCE FREQUENCY (TCXO) CONFIGURATION AND START UP PROCEDURE

After power up NT1068.2 assumes feeding with 10MHz TCXO signal and wakes up in the active mode. PLLs are supposed to be locked after 1 ms and generally chip is ready for operation in the following configuration:

- PLL “A” is set to L1 band and feeds Channel#1 and Channel#2 with LO = 1590 MHz
- PLL “B” is set to L2/L3/L5 band and feeds Channel#3 and Channel#4 with LO = 1235 MHz
- Channel#1 down converts lower sideband (i.e. L1 GPS/Galileo/BeiDou/QZSS)
- Channel#2 down converts upper sideband (i.e. L1 GLONASS)
- Channel#3 down converts upper sideband (i.e. L2 GLONASS)
- Channel#4 down converts lower sideband (i.e. L2 GPS/QZSS)
- All channels are set to analog differential output data interface, RF GC system in manual mode @ max gain, IF GC system in auto mode
- PLL “A” and PLL “B” tuning systems were executed
- 53 MHz CLK of differential type is pushed out

IF another TCXO is used, some actions should be performed in order to make NT1068.2 perform properly. Execution sequence is important and described below:

- set Reg3 D[7–1] to desired TCXO frequency (select frequency range to which TCXO frequency belongs)
- perform PLL “A” and PLL “B” (if intended to use) reconfiguration according to sections 7.3 and 7.4 to get desired LO frequency

Reference frequency indicator shows whether TCXO is connected to NT1068.2 (Reg7 D[5] = “0”) or not (Reg7 D[5] = “1”).

7.2. FREQUENCY BAND SELECTION

To work with specific configurations, select desired frequency bands for PLL “A” and “B” according to guidelines given below:

- to downconvert signals of S+L2 bands with single PLL:
  - write “11” to Reg41 D[2–1] – PLL “A” will be set to feed Channel#1 with LO signal of S band (e.g. 2480MHz) and Channel#2 with LO signal of L2 band (e.g. 1240MHz)
- to downconvert signals of L1+L3/L5 bands with single PLL:
  - write “11” to Reg45 D[2–1] – PLL “B” will be set to feed Channel#3 with LO signal of L1 band (e.g. 1590MHz) and Channel#4 with LO signal of L3/L5 band (e.g. 1192.5MHz)
- to downconvert signals of L1+L3+L5 bands with single PLL:
  - write “10” to Reg45 D[2–1] – PLL “B” will be set to feed Channel#3 with LO signal of L1 band (e.g. 1590MHz); Channel#1 and Channel#4 with LO signals of L3+L5 band (e.g. 1192.5MHz)
- to acquire signals E6 and E1+E5a+E5b with single chip:

- write “10” to Reg41 D[2–1] – PLL “A” will be set to feed only Channel#2 with LO signal of E6 band (e.g. 1260MHz)
- write “10” to Reg45 D[2–1] – PLL “B” will be set to feed Channel#3 with LO signal of L1 band (e.g. 1590MHz); Channel#1 and Channel#4 with LO signals of L3+L5 band (e.g. 1192.5MHz)

After frequency bands are selected, refer to next section to calculate F_{LO} and divider ratio values.

7.3. PLL “A”/ PLL “B” RECONFIGURATION

In order to reconfigure PLL following procedure is recommended:

– for operating in L2/L3/L5 or L1 band (Reg41 D[2–1] is set to “00”, “01” or “10” / Reg45 D[2–1] is set to “00” or “01”):
  - using the formula: $F_{LO\_L} = \frac{N*F_{TCXO}}{R}$ choose ***N*** and ***R***
  - write ***N*** value to Reg42/Reg46 D[7–0] + Reg43/Reg47 D[7]
  - write ***R*** value to Reg43/Reg47 D[6–3]
  - execute tuning procedure – Reg43/Reg47 D[0]

– for operating in “S for ch#1 + L2 for ch#2” mode (Reg41 D[2–1] is set to “11”):
  - using the formula: $F_{LO\_S} = \frac{2*N*F_{TCXO}}{R}$ and $F_{LO\_L2} = \frac{N*F_{TCXO}}{R}$ choose common ***N*** and ***R*** for PLL “A”
  - write ***N*** value to Reg42 D[7–0] + Reg43 D[7]
  - write ***R*** value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]

– for operating in “L1 for ch#3 + L3&L5 for ch#1&4” or “L1 for ch#3 + L3/L5 for ch#4” modes (Reg45 D[2–1] is set to “10” or “11”):
  - using the formula: $F_{LO\_L1} = \frac{N*F_{TCXO}}{R}$ and $F_{LO\_L3/L5} = \frac{6*N*F_{TCXO}}{8*R}$ choose common ***N*** and ***R*** for PLL “B”
  - write ***N*** value to Reg46 D[7–0] + Reg47 D[7]
  - write ***R*** value to Reg47 D[6–3]
  - execute tuning procedure – Reg47 D[0]

In PLL “A” only mode (Reg2 D[1–0] is set to “01” or “10”) it is recommended to set Reg41 D[2–1] to “00” or “01” and reconfigure PLL “A” according to the sequence given above if needed.

To halve F_{LO} step without changing F_{PFD}, use the following formula to calculate ***N***, ***n*** and ***R*** values, where ***n*** is Reg43/Reg47 D[2]:

– $F_{LO\_L} = \frac{(2N+n)*F_{TCXO}}{2*R}$

– $F_{LO\_S} = \frac{2*(2*N+n)*F_{TCXO}}{2*R}$ and $F_{LO\_L2} = \frac{(2*N+n)*F_{TCXO}}{2*R}$

– $F_{LO\_L1} = \frac{(2*N+n)*F_{TCXO}}{2*R}$ and $F_{LO\_L3/L5} = \frac{6*(2*N+n)*F_{TCXO}}{2*8*R}$

7.4. SINGLE LO SOURCE CONFIGURATION

In order to switch to single LO mode following actions are to perform:

– set Reg3 D[0] to “0” to feed all mixers from PLL “A”
– turn off PLL “B” by setting Reg45 D[0] to “0”

- for feeding channels with L2/L3/L5 or L1-band LO (Reg41 D[2–1] is set to “00” or “01”):
  - using the formula: $F_{LO\_L} = \frac{N * F_{TCXO}}{R}$ choose ***N*** and ***R***
  - write ***N*** value to Reg42 D[7–0] + Reg43 D[7]
  - write ***R*** value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]
- for feeding all channels with S-band LO (Reg41 D[2–1] is set to “10”):
  - using the formula: $F_{LO\_S} = \frac{2 * N * F_{TCXO}}{R}$ choose ***N*** and ***R***
  - write ***N*** value to Reg42 D[7–0] + Reg43 D[7]
  - write ***R*** value to Reg43 D[6–3]
  - execute tuning procedure – Reg43 D[0]

7.5. POWER SUPPLY OPTIONS

Specified range of supply voltage is from 1.8V ±5% to 3.3V ±10%. There is supply voltage level indicator showing that it is higher than 2.85V (Reg7 D[3]=“0”) or lower (Reg7 D[3]=“1”).

Supply voltage higher than 2.85V must be applied to common pin IC_VCC (pin #36 of the QFN88 package).

If supply voltage is 1.8V ±5%:
- set Reg2 D[4] = “0” to apply 1.8V to common pin IC_VCC;
- set Reg2 D[4] = “1” to apply 1.8V directly to each block.

When high performance is not needed (e.g. for tracking mode) NT1068.2 can be ‘on-fly’ switched to ECO mode by setting Reg2 D[2] = “1” to reduce power consumption. Some parameters will degrade, please refer to section 5.

7.6. SUPPLY VOLTAGE MONITORING AND SOFTWARE RESET

Supply voltage failure indicator (SVFI) is intended to inform about occurred supply voltage reset that led to registers reset to default values. SVFI is available in Reg7 D[2] and is in “0” state by default. In order to work with SVFI perform the following actions:
- write “1” to Reg7 D[2];
- permit SVFI as AOK’s component – write “1” to Reg6 D[6].

If during the operation AOK is “0”, check SVFI state:
- if SVFI is fail (Reg7 D[2] is “0”), i.e. registers were reset to default states:
  - write desired configuration file to IC;
  - execute PLLs tuning procedure – Reg43/Reg47 D[0];
  - write “1” to Reg7 D[2];
  - permit SVFI as AOK’s component – write “1” to Reg6 D[6];
- if SVFI is valid (Reg7 D[2] is “1”):
  - perform software reset – write “1” to Reg2 D[3], i.e. registers will be reset to default states;
  - finish software reset – write “0” to Reg2 D[3];
  - write desired configuration file to IC;
  - execute PLLs tuning procedure – Reg43/Reg47 D[0];
  - write “1” to Reg7 D[2];
  - permit SVFI as AOK’s component – write “1” to Reg6 D[6].

7.7. SPLITTER CONFIGURATION

Internal 1-to-n RF splitter (n=1,2,3,4) with configurable channel combination can be used along with separate RF inputs for other channels. In order to work with splitter input, enable desired channels (write "1" to Reg 13 D[0] for Channel#1 / Reg20 D[0] for Channel#2 / Reg27 D[0] for Channel#3 / Reg34 D[0] for Channel#4) and select splitter mode for each channel dedicated to splitter input (write "1" to Reg 13 D[2] for Channel#1 / Reg20 D[2] for Channel#2 / Reg27 D[2] for Channel#3 / Reg34 D[2] for Channel#4). Enabled channels that are not set to splitter mode can be supplied with RF signal via RF#_IN pins.

7.8. RF AGC CONFIGURATION

RF GC system of NT1068.2 starts in the manual operation mode. You can change RF gain value manually by setting corresponding value with Reg17 D[7–4] for Channel#1 / Reg24 D[7–4] for Channel#2 / Reg31 D[7–4] for Channel#3 / Reg38 D[7–4] for Channel#4.

Actual RF power detector status is available at Reg9 D[5–4] in both manual and automatic modes. Reg9 D[5] indicates the crossing of upper threshold and Reg9 D[4] indicates the crossing of lower one. The thresholds are corresponding to the definite level of output power of input stage that's why they depend on RF Gain value. The thresholds' values in section 4.4.2.4 are shown for max RF Gain settings (code "1111" is written to Reg17 D[7–4] for Channel#1 / Reg24 D[7–4] for Channel#2 / Reg31 D[7–4] for Channel#3 / Reg38 D[7–4] for Channel#4). To calculate the actual dBm-value of the threshold please use the equation:

$$TH_{ACT} = TH_{GTmax} + GT_{MAX} - GT_{SET},$$

where

TH_{ACT} – actual threshold value, dBm;
TH_{GTmax} – threshold value for max RF Gain (shown in reg description table), dBm;
GT_{MAX} - maximum RF Gain, dB.
GT_{SET} – actual RF Gain, chosen by settings, dB.

An upper threshold could be adjusted by Reg16 D[7–4] for Channel#1 / Reg23 D[7–4] for Channel#2 / Reg30 D[7–4] for Channel#3 / Reg37 D[7–4] for Channel#4. A lower threshold could be adjusted by Reg16 D[3–0] for Channel#1 / Reg23 D[3–0] for Channel#2 / Reg30 D[3–0] for Channel#3 / Reg37 D[3–0] for Channel#4. Power values shown in registers description table are calculated with respect to input signal power. The upper threshold should always be higher than lower. Also it is strongly recommended to set dBm-value of upper threshold at least 3dB higher than lower threshold to guarantee stability of RF AGC loop.

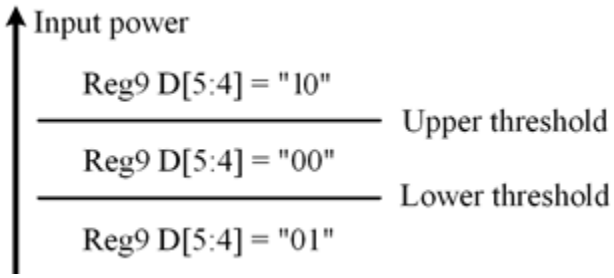


Figure 7.1: RF AGC power detector status operation logic

The RF AGC thresholds can be changed in order to improve RF channel linearity by decreasing dBm value of both thresholds (IM3 will increase since each block will operate with weaker input signal) or to improve RF channel noise figure by increasing thresholds' dBm value (noise of

channel blocks will be more suppressed by higher gain of input amplifier and SNR of the receiver will be improved).
To enable automatic mode the Reg15 D[4] for Channel#1 / Reg22 D[4] for Channel#2 / Reg29 D[4] for Channel#3 / Reg36 D[4] for Channel#4 should be switched to "1". While automatic mode enabled, the RF AGC system will adjust the RF gain to keep its output power between RF AGC thresholds.
The status of RF gain control register is available at Reg9 D[3–0].

7.9. IF AGC THRESHOLD CONFIGURATION

If 400mV (w.r.t. sine wave signal) option is chosen for output peak-to peak voltage (Reg15 D[6] for Channel#1 / Reg22 D[6] for Channel#2 / Reg29 D[6] for Channel#3 / Reg36 D[6] for Channel#4) it is recommended not to solder terminating 200 Ohm resistor and to write appropriate values ("0") to D[5] of the same registers. It will result in slightly better intermodulation performance; however, channel bandwidth will be narrower.

7.10. 2-BIT ADC CONFIGURATION

After power up NT1068.2 is preconfigured to analog differential output data interface. However, there is an option to set up 2-bit ADC outputs in Reg15 D[0] for Channel#1 / Reg22 D[0] for Channel#2 / Reg29 D[0] for Channel#3 / Reg36 D[0] for Channel#4.

2-bit ADCs output type can be CMOS or LVDS (Reg19 D[4] for Channel#1 / Reg26 D[4] for Channel#2 / Reg33 D[4] for Channel#3 / Reg40 D[4] for Channel#4).

Table 7.1: 2-bit ADC and clock outputs

	CMOS		LVDS	
Channel #1	Pin #71 - MAGN	Pin #70 - SIGN	Pin #71 - Complement	Pin #70 - True
Channel #2	Pin #62 - MAGN	Pin #63 - SIGN	Pin #62 - Complement	Pin #63 - True
Channel #3	Pin #49 - MAGN	Pin #48 - SIGN	Pin #49 - Complement	Pin #48 - True
Channel #4	Pin #40 - MAGN	Pin #41 - SIGN	Pin #40 - Complement	Pin #41 - True
Clock output		Pin #56 - CMOS	Pin #55 - Complement	Pin #56 - True

In CMOS mode logic-level high setting depends on supply voltage level and can be changed in Reg19 D[1-0] for Channel#1 / Reg26 D[1-0] for Channel#2 / Reg33 D[1-0] for Channel#3 / Reg40 D[1-0] for Channel#4.

In LVDS mode the same bits are intended to control ADC output current. In ECO mode ADC output current on the same setting will be lower.

LVDS clock output type must be enabled when channel output data interface is 2-bit ADC and ADC output type is LVDS. LVDS clock output peak-to-peak voltage setting must be the same as ADC output current setting, e.g. "10" is set by default.

2-bit ADCs are able to operate in one of three modes:
- clocked by rising edge;
- clocked by falling edge;
- asynchronous (available for CMOS output only).

These modes can be set up in Reg19 D[3–2] for Channel#1 / Reg26 D[3–2] for Channel#2 / Reg33 D[3–2] for Channel#3 / Reg40 D[3–2] for Channel#4.

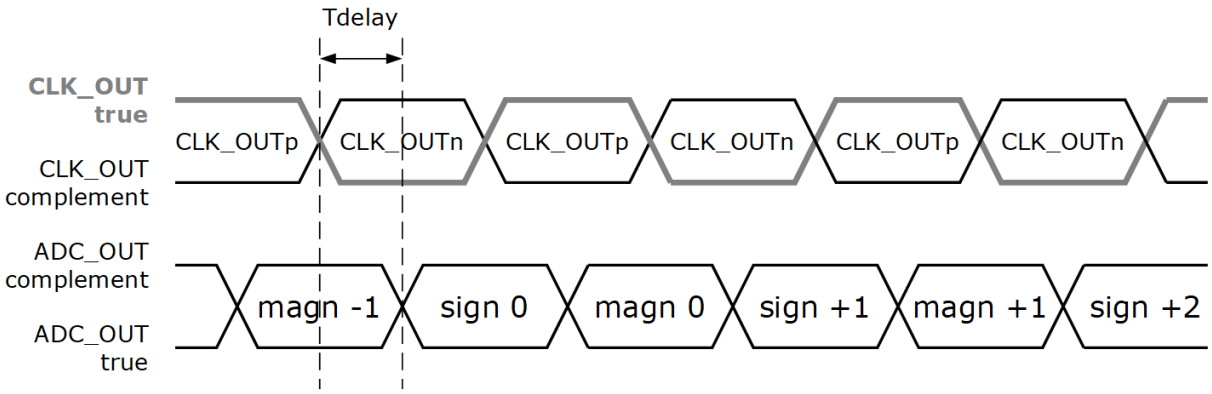


Figure 7.2: ADC data sampling in LVDS mode

Typical Tdelay is 4.4ns. For ADCs clock frequency information, please, refer to section 7.11.

In “asynchronous” mode 2-bit ADCs act as voltage level comparators so no any clocking applied. For example, this mode may be use full if several NT1068.2s should operate simultaneously pushing out digitized data that can be synchronized with single clock on correlator and processor side.

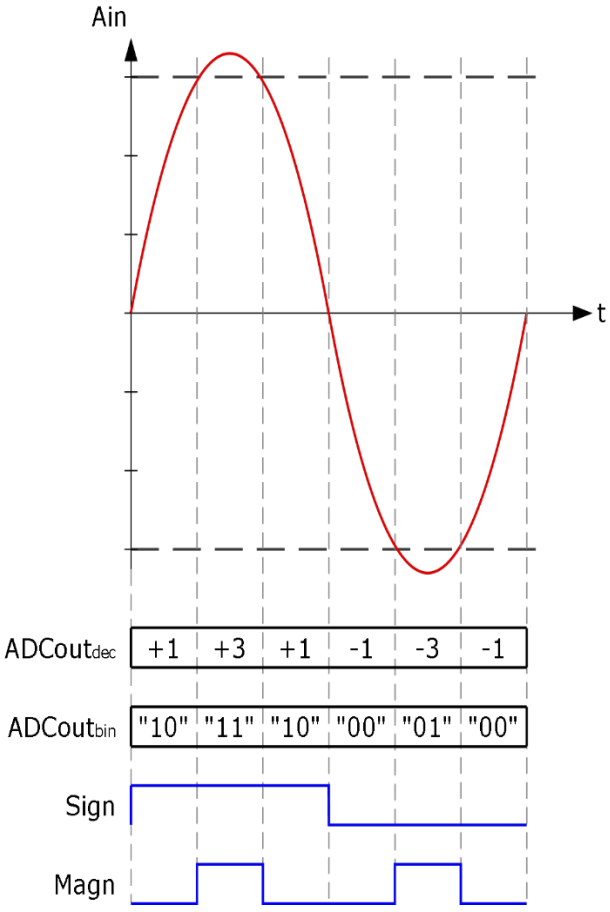


Figure 7.4: ADC quantization levels (sinewave signal example)

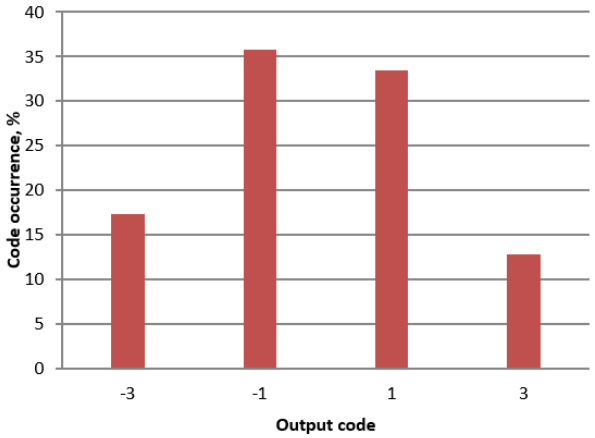


Figure 7.3: Typical channel histogram (2-bit ADC output)

7.11. CLK FREQUENCY CONFIGURATION

CLK signal is intended for clocking all 2-bit ADCs as well as clocking external correlator engine. It is generated from LO frequency either from PLL "A" or PLL "B" (set Reg12 D[6–5] to "00" or "01" respectively) or is taken from TCXO (set Reg12 D[6–5] to "11").

If clock is generated from PLL "A" or "B" its frequency can be customized by procedure:

- choose CLK source by setting appropriate value to Reg12 D[6–5]
- if operating in L2/L3/L5 or L1 band (Reg3 D[0] is set to "0" or "1" and Reg41 D[2–1] is set to "00", "01" or "10" / Reg45 D[2–1] is set to "00" or "01"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L}}{2*C}$ choose $\boldsymbol{C}$
  - write $\boldsymbol{C}$ value to Reg11 D[4–0]
- if operating in S+L2 bands (Reg3 D[0] is set to "1" and Reg41 D[2–1] is set to "11"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L2}}{2*C}$ and $F_{CLK} = \frac{F_{LO\_S}}{4*C}$ choose common $\boldsymbol{C}$
  - write $\boldsymbol{C}$ value to Reg11 D[4–0]
- if operating in L1+L3/L5 bands or L1+L3+L5 (Reg3 D[0] is set to "1" and Reg45 D[2–1] is set to "10" or "11"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_L1}}{2*C}$ and $F_{CLK} = \frac{2*F_{LO\_L3/L5}}{3*C}$ choose common $\boldsymbol{C}$
  - write $\boldsymbol{C}$ value to Reg11 D[4–0]
- if operating in S band (Reg3 D[0] is set to "0" and Reg41 D[2–1] is set to "10"):
  - using the formula: $F_{CLK} = \frac{F_{LO\_S}}{4*C}$ choose $\boldsymbol{C}$
  - write $\boldsymbol{C}$ value to Reg11 D[4–0]

To halve F_{CLK} step without changing F_{LO}, use the following formula to calculate $\boldsymbol{C}$ and $\boldsymbol{c}$ values, where $\boldsymbol{c}$ is Reg11 D[5]:

- $F_{CLK} = \frac{F_{LO\_L}}{2*C+c}$
- $F_{CLK} = \frac{F_{LO\_L2}}{2*C+c}$ and $F_{CLK} = \frac{F_{LO\_S}}{4*C+c}$
- $F_{CLK} = \frac{F_{LO\_L1}}{2*C+c}$ and $F_{CLK} = \frac{2*F_{LO\_L3/L5}}{3*C+c}$
- $F_{CLK} = \frac{F_{LO\_S}}{4*C+c}$

If clock is taken from TCXO (Reg12 D[6–5] is set to "11") it can be divided by 2, 4 or 8 (refer to Reg11 D[7–6] to select divider ratio value).

If Reg3 D[0] is set to "0" PLL "B" will be available only for generating CLK frequency.

If channel output data interface is analog or ADC is in asynchronous mode, CLK output can be disabled by setting Reg12 D[6–5] to "10".

7.12. CLK OUTPUT TYPE USAGE

Differential clock output type is set by default, its peak-to-peak voltage can be changed in Reg12 D[3-2], DC level – in Reg12 D[1-0] (depends on supply voltage level).

Besides differential, CMOS and LVDS clock output types are available.

In order to select CMOS clock output type, set Reg12 D[4] = "0". Logic-level high can be changed in Reg12 D[1-0] (depends on supply voltage level).

In order to select LVDS clock output type, set Reg12 D[7] = "1" and refer to Reg12 D[3-2] to change peak-to-peak voltage. In ECO mode peak-to-peak voltage on the same setting will be lower.

LVDS clock output type must be enabled when channel output data interface is 2-bit ADC and ADC output type is LVDS (Reg15 D[0] for Channel#1 / Reg22 D[0] for Channel#2 / Reg29 D[4] for Channel#3 / Reg36 D[0] for Channel#4 is set to "1" and Reg19 D[4] for Channel#1 / Reg26 D[4] for Channel#2 / Reg33 D[4] for Channel#3 / Reg40 D[4] for Channel#4 is set to "1"). LVDS clock output peak-to-peak voltage setting must be the same as ADC output current setting, e.g. "10" is set by default.

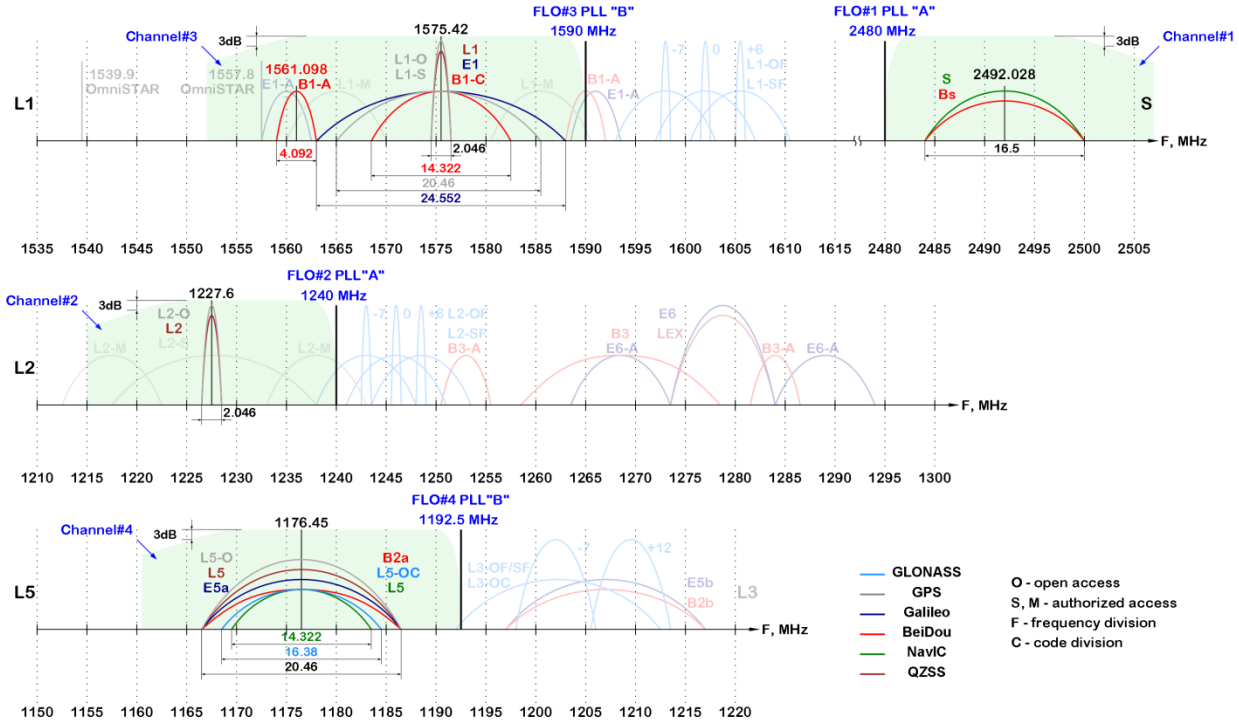
Choosing frequency plan, clock frequency, its output type and amplitude, pay attention to appearing of interferences at the LNA#_IN pins and then down converting to IF band. These interferences are caused by CLK signal harmonics and allocated frequencies can be calculated as $F_{jam} = N * F_{CLK}, N = 1,2,3,4 \ldots$

7.13. TEMPERATURE MEASUREMENT PROCEDURE

Two modes of temperature modes are available: single and continuous (Reg5 D[1]). In single mode the measurement is done once upon request to Reg5 D[0] by setting "1" and result will be stored in Reg7 D[1–0] + Reg8 D[7–0] after procedure is finished (auto reset to "0" in Reg5 D[0] indicates this) until next execution. One temperature measurement procedure time is up to 17 ms. To enter in continuous mode set Reg5 D[1] to "1" first then execute with Reg5 D[0]. In this case embedded temperature sensor periodically runs the measurement procedure and only the latest result is stored in Reg7 D[1–0] + Reg8 D[7–0]. In order to stop continuous execution Reg5 D[1] should be set to "0".

7.14. OPERATION EXAMPLES

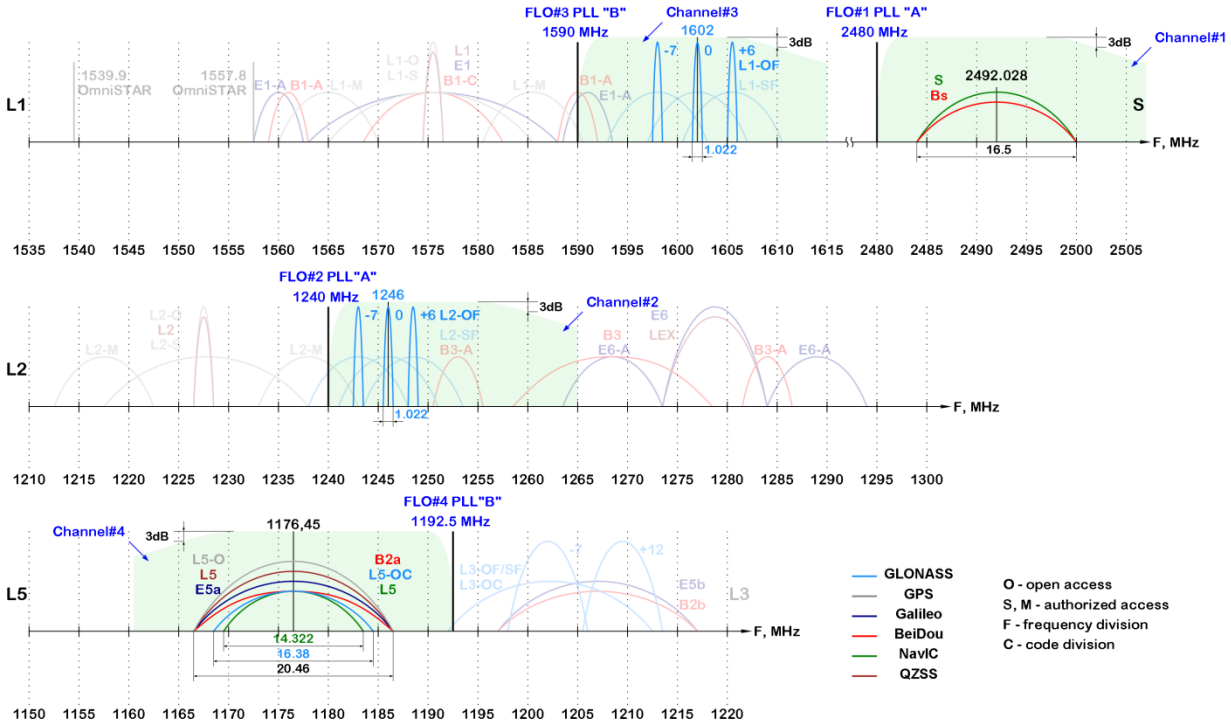
7.14.1. CONFIGURATION SET #1



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	68.9 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Lower sideband (GPS L2, QZSS L2)
Ch#3 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	33 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	2480 MHz
F_{LO}#2 PLL “A”	1240 MHz
F_{LO}#3 PLL “B”	1590 MHz
F_{LO}#4 PLL “B”	1192.5 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#1”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

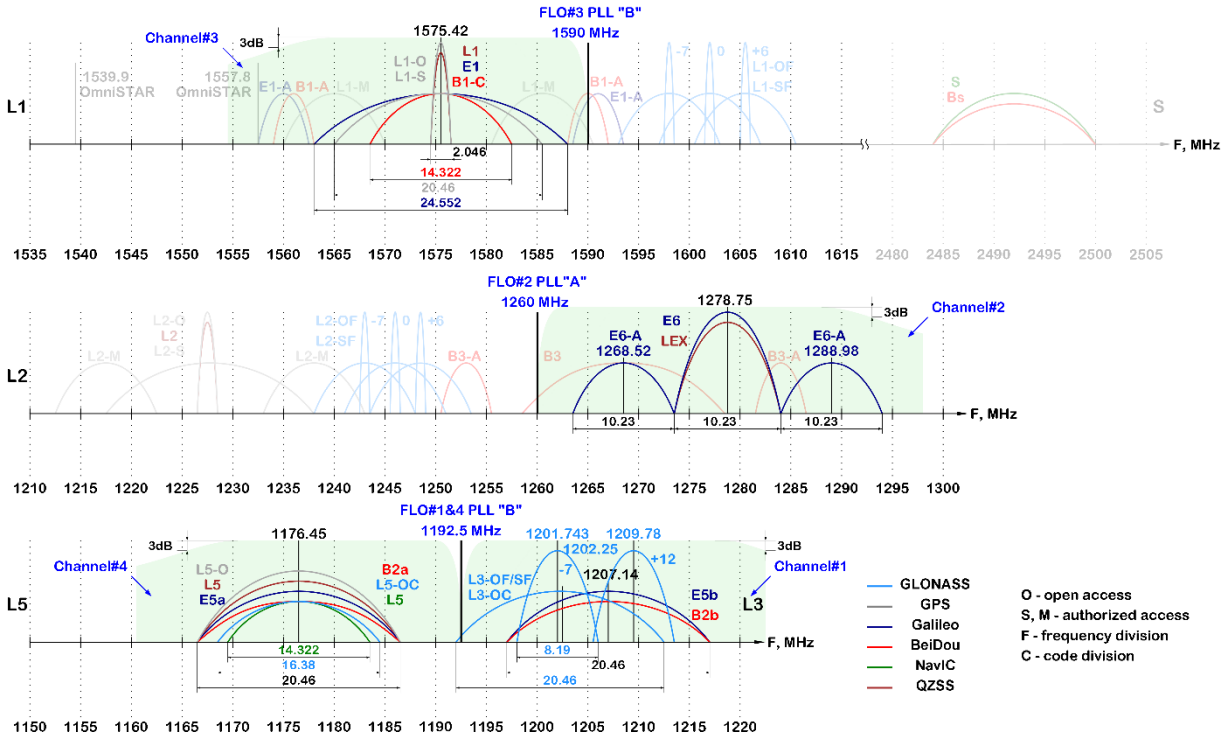
7.14.2. CONFIGURATION SET #2



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	62 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Upper sideband (GLONASS L2)
Ch#3 GNSS	Upper sideband (GLONASS L1)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	20 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	2480 MHz
F_{LO}#2 PLL “A”	1240 MHz
F_{LO}#3 PLL “B”	1590 MHz
F_{LO}#4 PLL “B”	1192.5 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#2”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

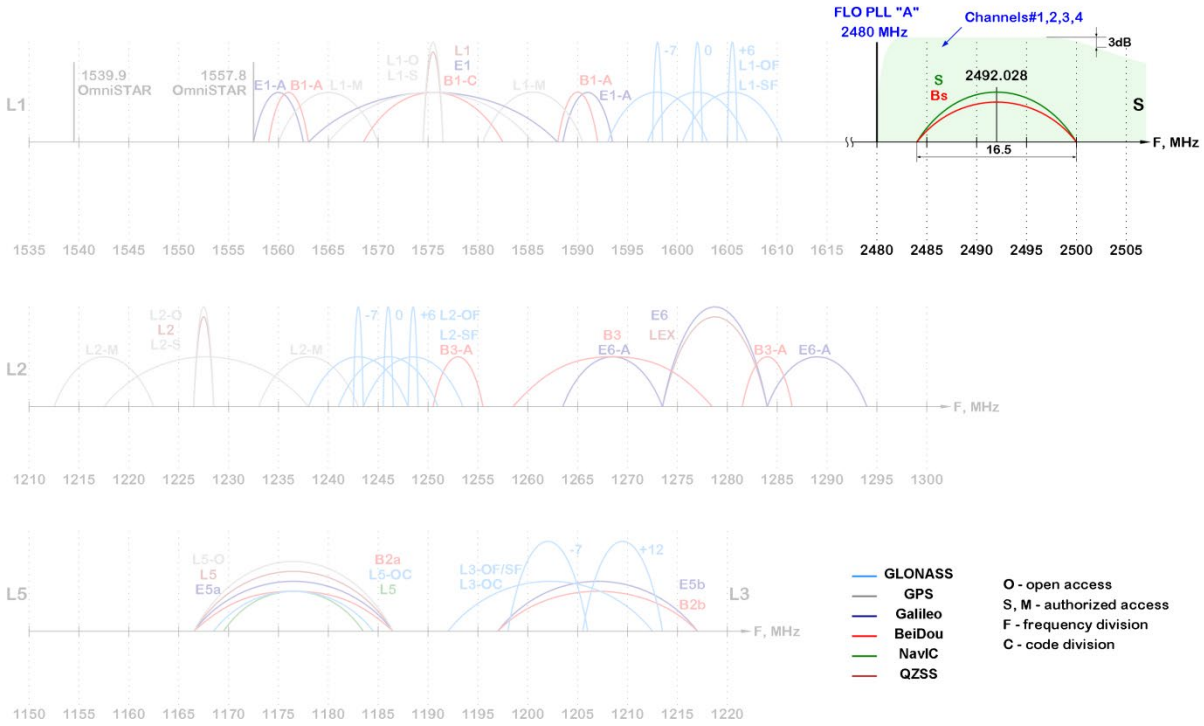
7.14.3. CONFIGURATION SET #3



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#2 PLL “B” for ch#1, ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	70 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#2 GNSS	Upper sideband (Galileo E6 and E6-A, QZSS LEX)
Ch#3 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30 MHz
Ch#2 IF passband	33 MHz
Ch#3 IF passband	31 MHz
Ch#4 IF passband	27 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO}#1 PLL “A”	1192.5 MHz
F_{LO}#2 PLL “A”	1260 MHz
F_{LO}#3 PLL “B”	1590 MHz
F_{LO}#4 PLL “B”	1192.5 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#3”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

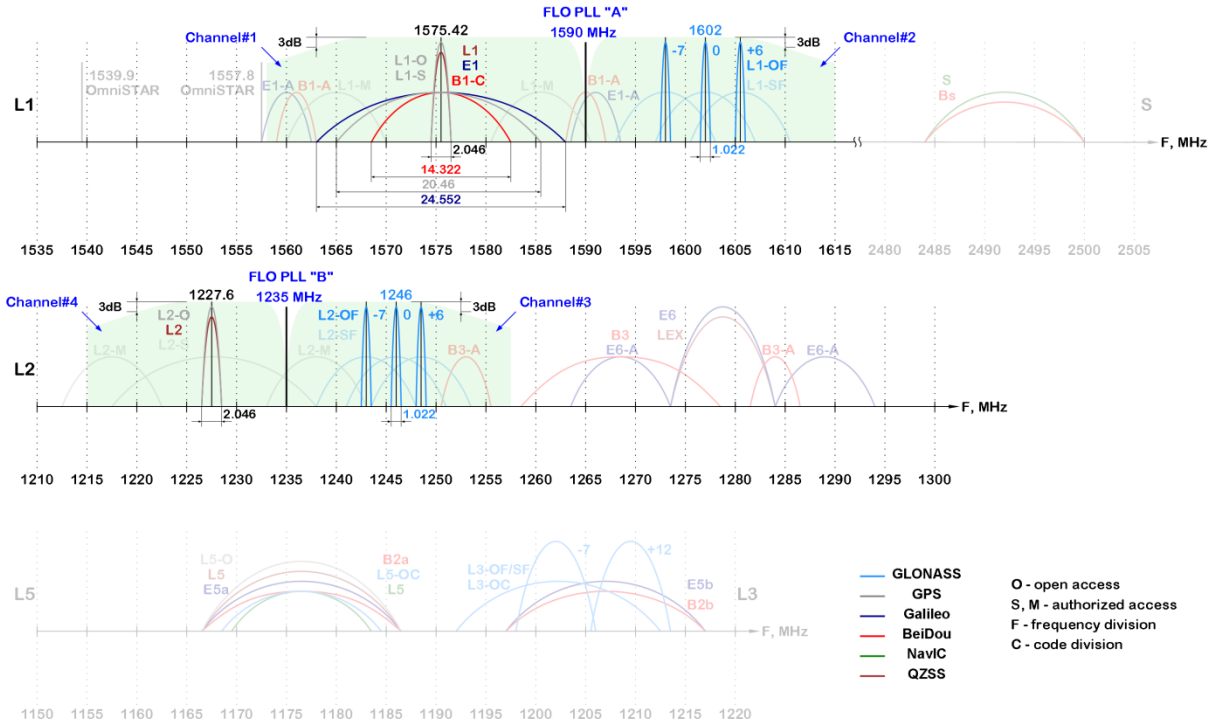
7.14.4. CONFIGURATION SET #4



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for all channels
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	47.7 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#2 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#3 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#4 GNSS	Upper sideband (NavIC S, BeiDou Bs)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	22 MHz
Ch#3 IF passband	22 MHz
Ch#4 IF passband	22 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	2480 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#4”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

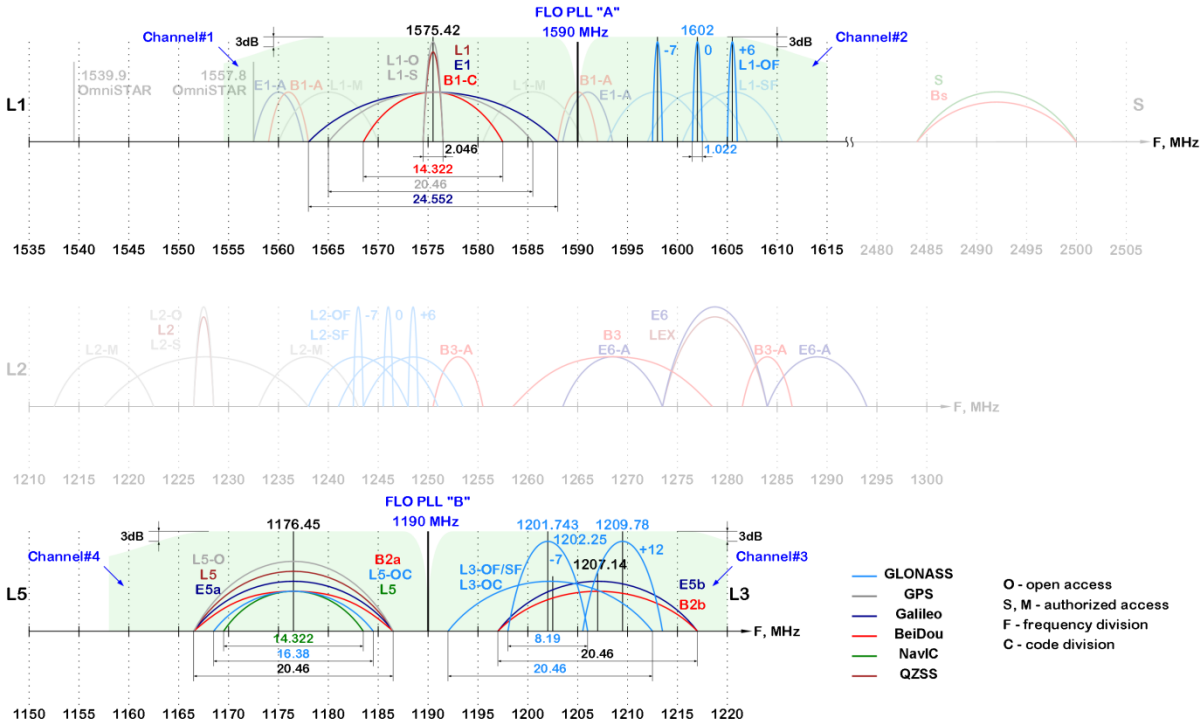
7.14.5. CONFIGURATION SET #5



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	61.2 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Upper sideband (GLONASS L1)
Ch#3 GNSS	Upper sideband (GLONASS L2)
Ch#4 GNSS	Lower sideband (GPS L2, QZSS L2)
Ch#1 IF passband	27 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	17.5 MHz
Ch#4 IF passband	15 MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1235 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#5”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

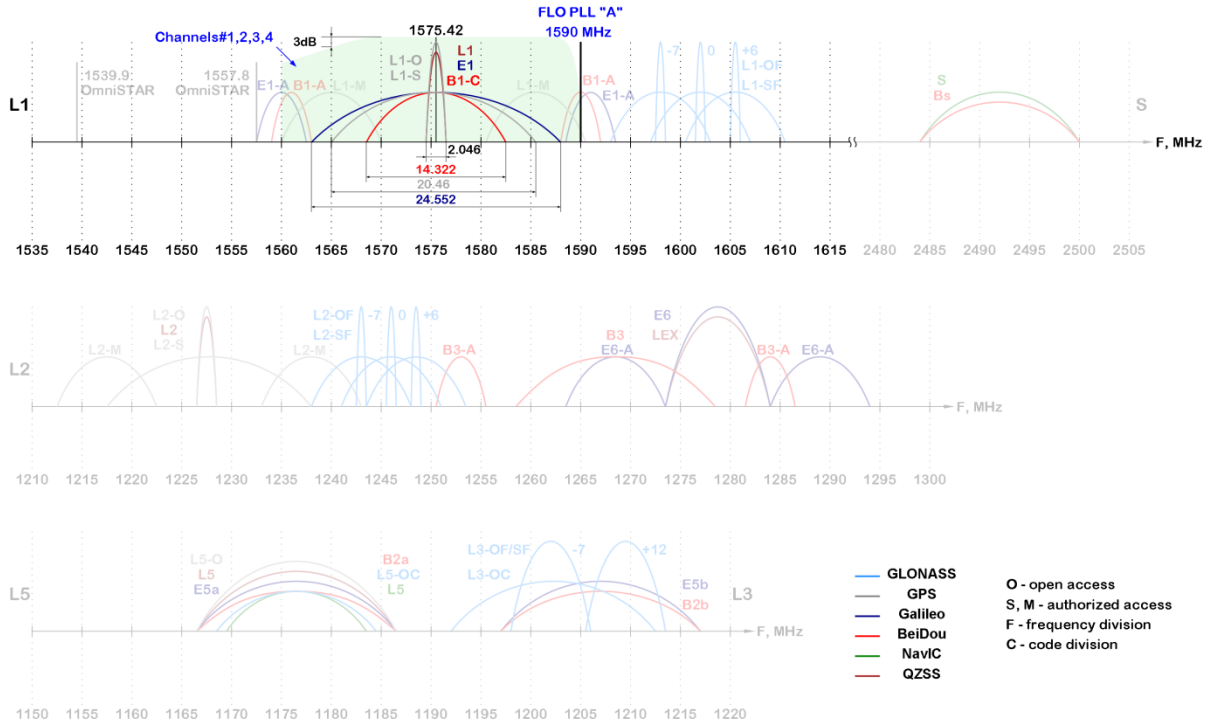
7.14.6. CONFIGURATION SET #6



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	61.2 MHz
CLK output type	CMOS
CLK output amplitude	Ext. (VCC)
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Upper sideband (GLONASS L1)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30.5 MHz
Ch#2 IF passband	20 MHz
Ch#3 IF passband	30 MHz
Ch#4 IF passband	27MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1190 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#6”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

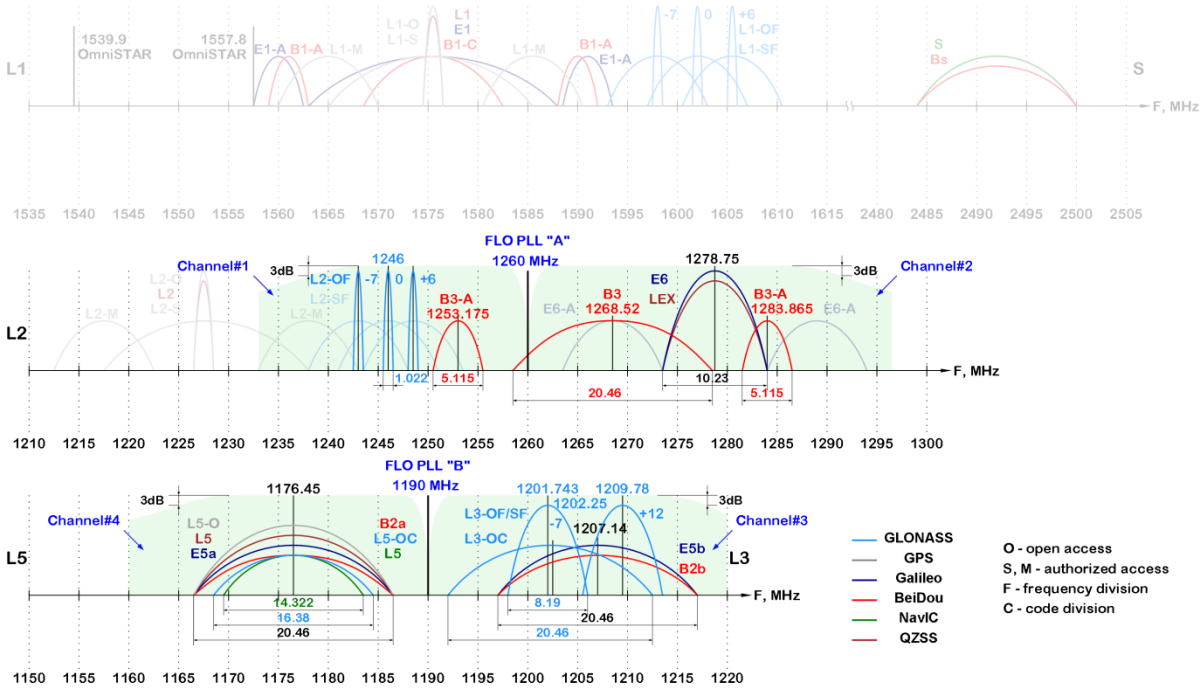
7.14.7. CONFIGURATION SET #7



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for all channels
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	49.7 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#2 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#3 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#4 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#1 IF passband	25 MHz
Ch#2 IF passband	25 MHz
Ch#3 IF passband	25 MHz
Ch#4 IF passband	25 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	1590 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#7”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

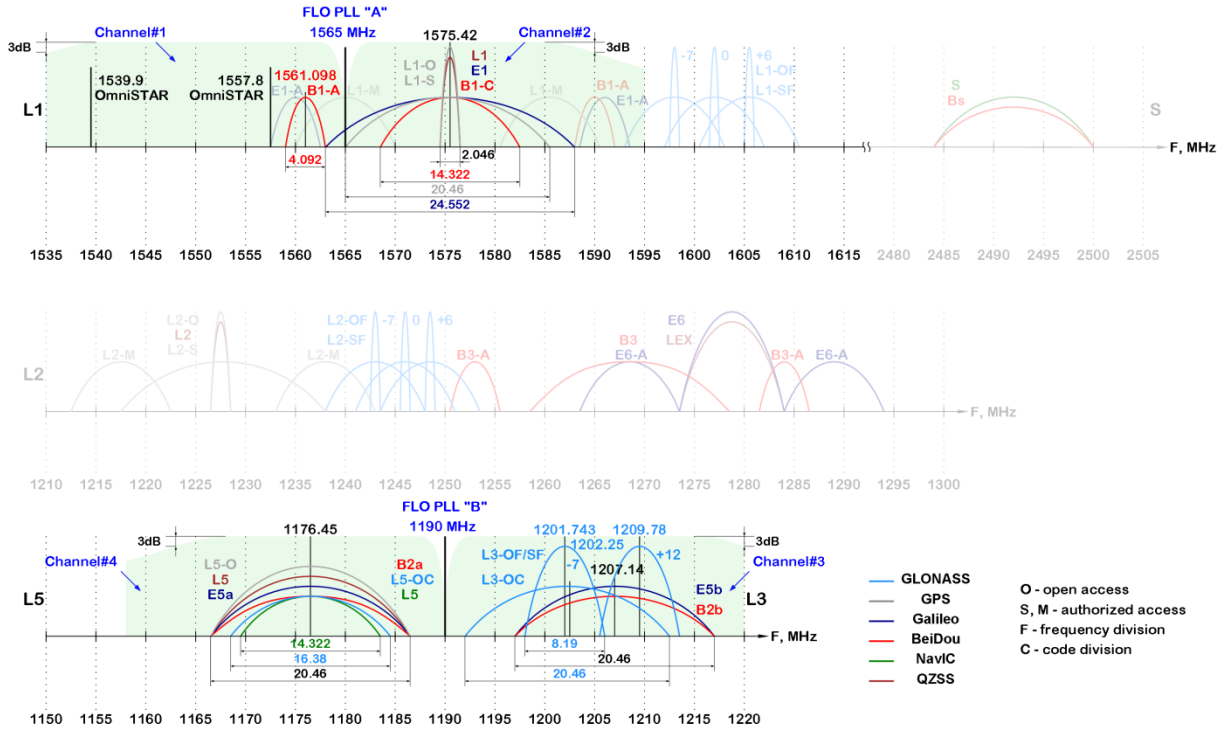
7.14.8. CONFIGURATION SET #8



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	57.3 MHz
CLK output type	Differential
CLK output amplitude	0.45V
Channel settings:	
Ch#1 GNSS	Lower sideband (GLONASS L2, BeiDou B3-A)
Ch#2 GNSS	Upper sideband (BeiDou B3, Galileo E6, QZSS LEX)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	22 MHz
Ch#2 IF passband	32 MHz
Ch#3 IF passband	28 MHz
Ch#4 IF passband	25 MHz
Output data interface	Analog differential
GC mode	RF manual + IF auto
IF AGC threshold	200mV
ADC output logic-level high	–
ADC type	–
PLL settings:	
F_{LO} PLL “A”	1260 MHz
F_{LO} PLL “B”	1190 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#8”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

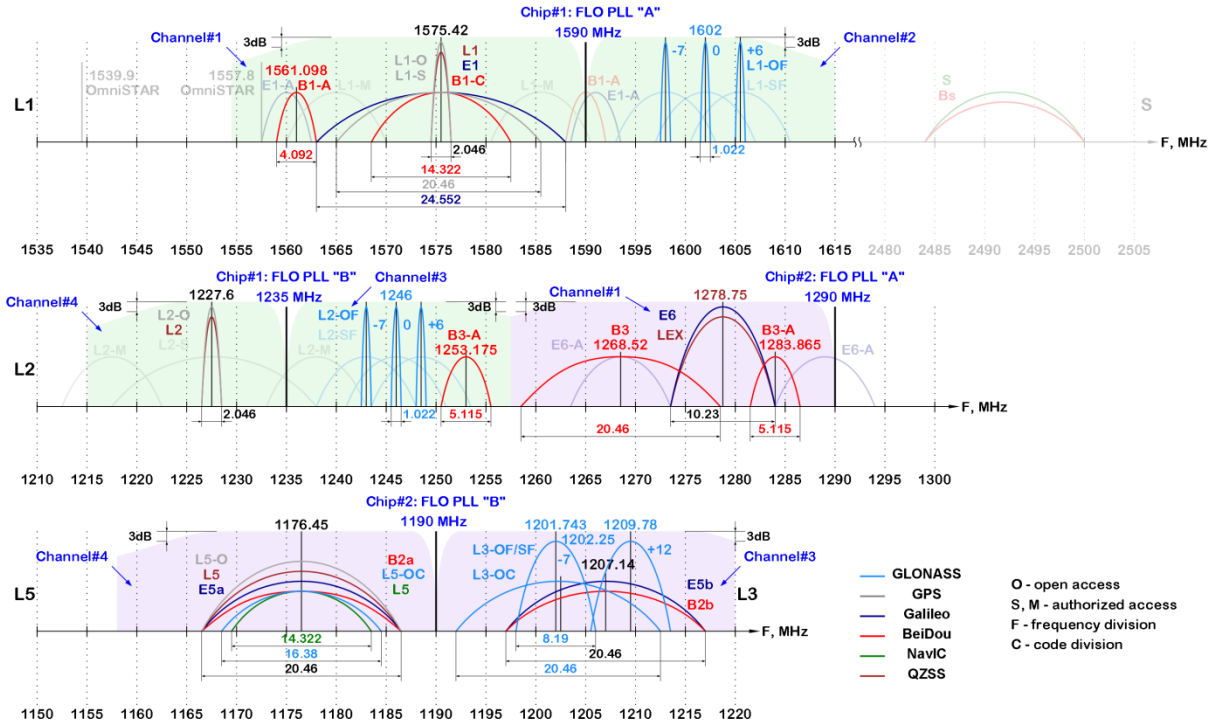
7.14.9. CONFIGURATION SET #9



General settings:	
Reference frequency (TCXO)	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	60.2 MHz
CLK output type	CMOS
CLK output amplitude	Ext. (VCC)
Channel settings:	
Ch#1 GNSS	Lower sideband (OmniStar 1557.8MHz, OmniStar 1539.9MHz, BeiDou B1-A)
Ch#2 GNSS	Upper sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1-C)
Ch#3 GNSS	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30 MHz
Ch#2 IF passband	25 MHz
Ch#3 IF passband	30 MHz
Ch#4 IF passband	28 MHz
Output data interface	2-bit ADC
GC mode	RF manual + IF auto
IF AGC threshold	30%
ADC output logic-level high	Ext. (VCC)
ADC type	Clocked by rising edge
PLL settings:	
F_{LO} PLL “A”	1565 MHz
F_{LO} PLL “B”	1190 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#9”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

7.14.10. CONFIGURATION SET #10



General settings:	Chip#1	Chip#2
Reference frequency (TCXO)	10 MHz	10 MHz
LO source	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4	PLL “A” for ch#1, ch#2 PLL “B” for ch#3, ch#4
Channel settings:		
Ch#1 GNSS	Lower sideband (GPS L1, QZSS L1, Galileo E1, BeiDou B1)	Lower sideband (BeiDou B3, Galileo E6, QZSS LEX)
Ch#2 GNSS	Upper sideband (GLONASS L1)	–
Ch#3 GNSS	Upper sideband (GLONASS L2, BeiDou B3-A)	Upper sideband (GLONASS L3, Galileo E5b, BeiDou B2b)
Ch#4 GNSS	Lower sideband (GPS L2, QZSS L2)	Lower sideband (GPS L5, GLONASS L5, Galileo E5a, QZSS L5, BeiDou B2a, NavIC L5)
Ch#1 IF passband	30.5 MHz	31 MHz
Ch#2 IF passband	20 MHz	–
Ch#3 IF passband	21 MHz	30 MHz
Ch#4 IF passband	15 MHz	27 MHz
Output data interface	2-bit ADC	2-bit ADC
GC mode	RF manual + IF auto	RF manual + IF auto
IF AGC threshold	30%	30%
ADC output logic-level high	Ext. (VCC)	Ext. (VCC)
ADC type	Clocked by rising edge	Clocked by rising edge
PLL settings:		
F_{LO} PLL “A”	1590 MHz	1290 MHz
F_{LO} PLL “B”	1235 MHz	1190 MHz

Please, open attachment of this datasheet to download-> “NT1068_2_ConfigSet#10_1”, “NT1068_2_ConfigSet#10_2”*
*configuration file may be also uploaded to NT1068.2 under GUI if renamed to .hex

7.15. PCB LAYOUT RECOMMENDATIONS

7.15.1. RECOMMENDED LAND PATTERN FOR QFN88

NT1068.2 is easy-to-use and easy-to-implement solution where no special layout tricks required. Although common RF related layout techniques and information given below are recommended not to be ignored.

1) Analog power domain separated from digital domain is recommended to be allocated for NT1068.2.
2) EMI-RFI shielding are highly recommended above NT1068.2 and related stuff.
3) Wave impedance should be kept up in accordance to the following:

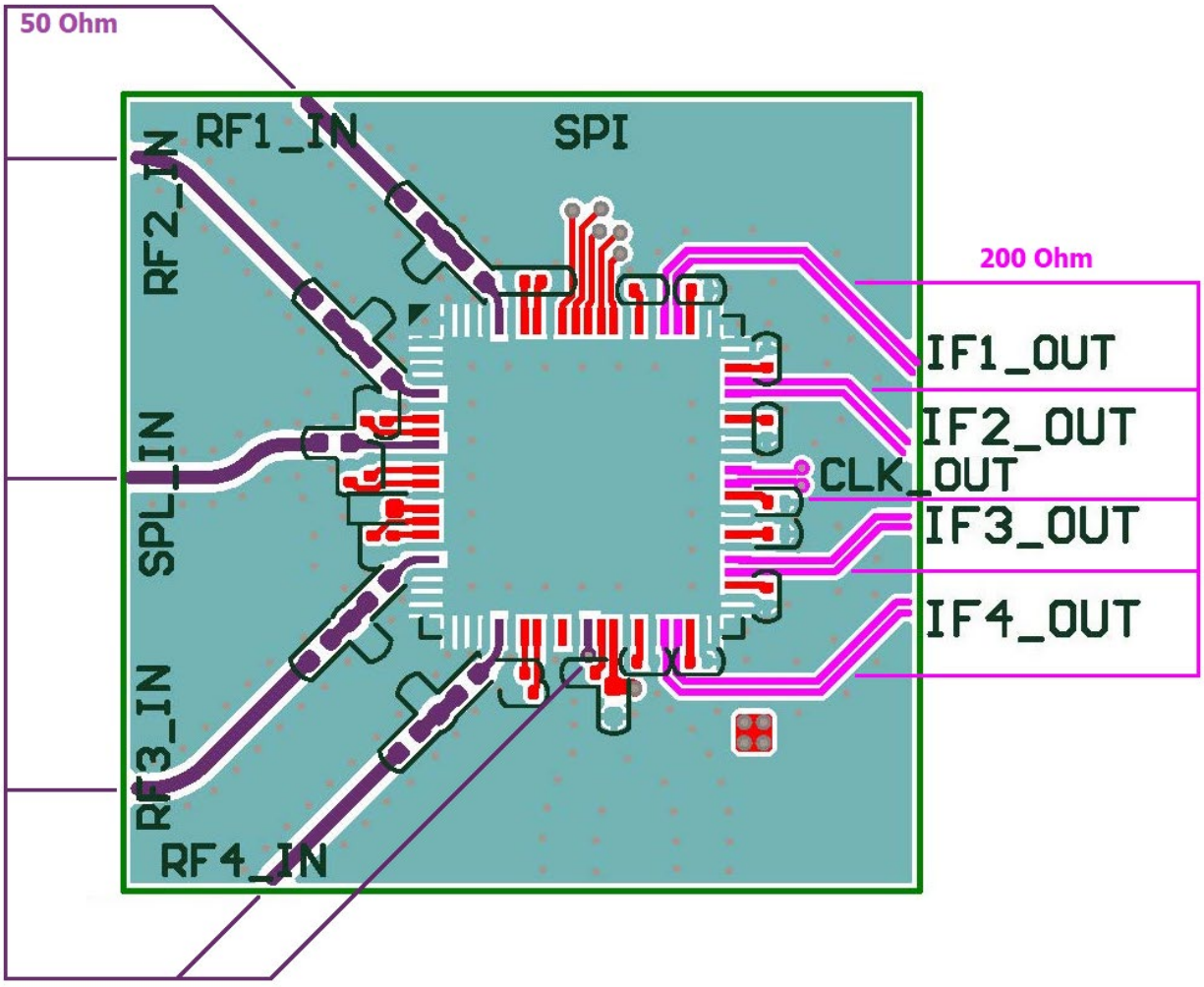


Figure 7.5: Recommended land pattern for QFN88

The violet traces on the Figure 7.5 should have 50 Ohm impedance and pink traces on the Figure 7.5 should have 200 Ohm impedance (if analog differential output).

7.15.2. RECOMMENDED STACK UP

LAYER	NAME OF LAYER	TYPE	THICKNESS mm	VIAS
1	EXTERNAL COPPER	18µm + GalvCu 35µm	0.053	
	INNERLAYER	RO4003C 0.203mm 18µm/18µm	0.203	
2	INNER FOIL	18µm	0.018	
	PREPREG	7628-45 (0,18mm)	0.18	
3	INNER FOIL	18µm	0.018	
	INNERLAYER	High Tg 0,51mm 18µm/18µm	0.51	
4	INNER FOIL	18µm	0.018	
	PREPREG	7628-45 (0,18mm)	0.18	
5	INNER FOIL	18µm	0.018	
	INNERLAYER	RO4003C 0.203mm 18µm/18µm	0.203	
6	EXTERNAL COPPER	18µm + GalvCu 35µm	0.053	
		THICKNESS (mm) ±10%	1.454	

Figure 7.6: Recommended Rogers stack up

NT1068.2 electric characteristics described in the datasheet were proven on this very stack up.

8. PACKAGE INFORMATION

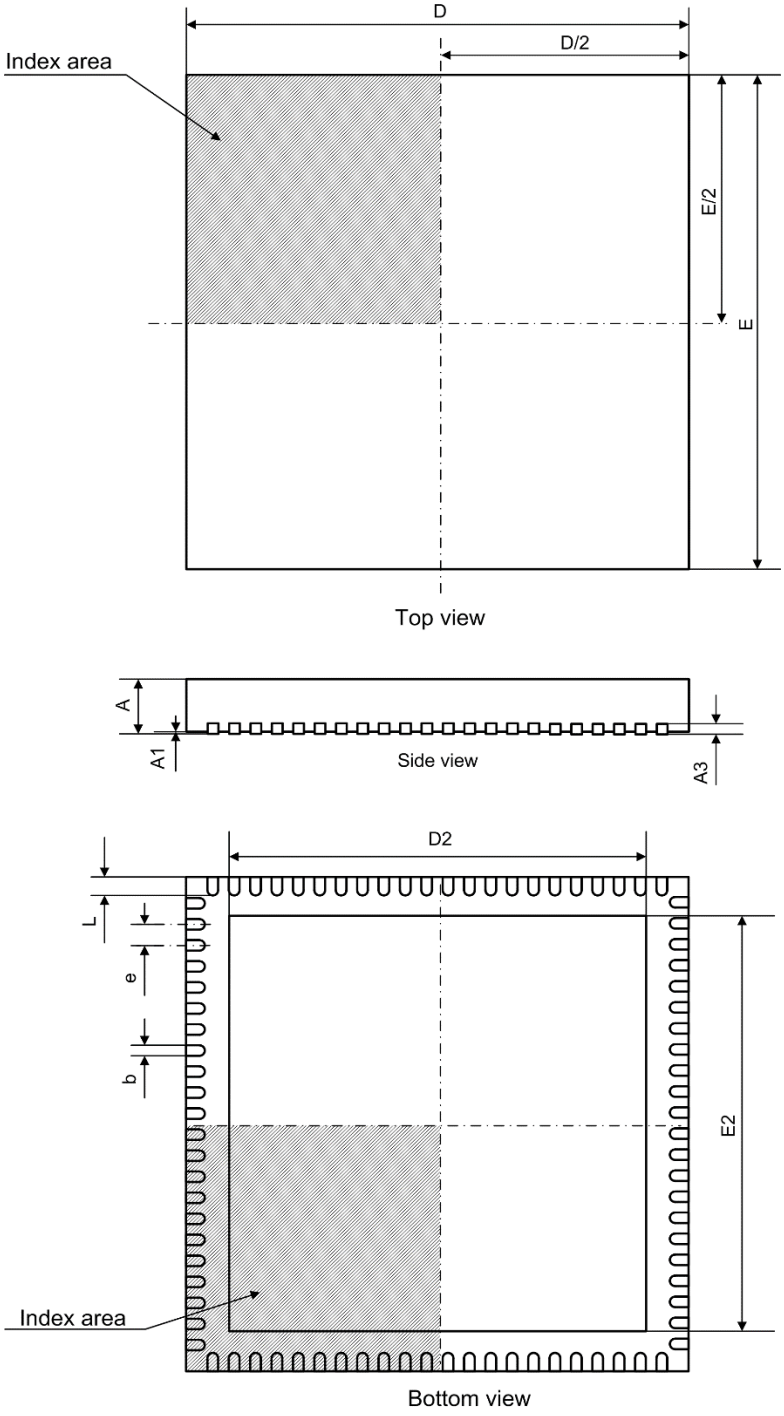


Figure 8.1: Package QFN88–10×10 [1]

Table 8.1: Package QFN88–10×10 dimensions[1]

Unit	A	A1	A3	b	D	D2	E	E2	e	L
min, mm	0.80	0.00	0.203 REF.	0.15	10.00 BSC	5.55	10.00 BSC	5.55	0.40 BSC	0.35
typ., mm	0.85	0.02		0.20		5.60		5.60		0.40
max, mm	0.90	0.05		0.25		5.65		5.65		0.45

[1] Package drawing and dimensions are for reference only. Actual values are compliant to JEDEC standard outlines MO–220.

9. REVISION HISTORY

From version 0.52 to 0.53:

- Attached file with recommended values updated

From version 0.51 to 0.52:

- Attached file with recommended values updated

From version 0.5 to 0.51:

- Subsection 4.4.2.2: Reg2, D [4] is service setting, do not change.
- Subsection 4.4.2.3: Reg12, D[7] renamed from “CLK_LVDS_MD” to “CLK_LVDS”

From version 0.4 to 0.5:

- Subsection 7.14: Attached configuration examples updated

From version 0.3 to 0.4:

- Subsection 5.1: IFA analog output DC level values updated
- Subsection 5.2: LO phase noise @ S band updated
- Subsection 4.2: Matching network elements added for E6 band
- Subsection 7.10: Application notes for LVDS mode updated