Multi-Channel GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS S/L1/L2/L3/L5 bands RF Front-End IC

1. OVERVIEW

NT1066 is a 4-channel RF Front-End IC (3 wideband IQ and 1 narrowband IQ) that covers simultaneously all GNSS (GLONASS, GPS, Galileo, BeiDou, QZSS, NavIC) signals at all frequency bands. It makes possible to benefit from all the advantages of acquiring multiple system simultaneously. Channels "A", "B" and "C" are designed with single conversion low-IF architecture, individually programmable and intended to receive L1, E1, B1, E6, B3, L2, L3, B2, L5, E5 in various combinations. IQ and image suppression modes are available, other options can be discovered in feature list. Channel "D" is dedicated to operate in S band or L2, L3, L5 bands of GNSS and has zero-IF architecture. S and L5 bands combining lets user to eliminate effectively ionospheric distortion utilizing large signal base. As alternative, channel "D" can be 'on a fly' software-reconfigured to receive real-time corrections data transmitted over FM, VHF and UHF bands.
NT1066 does also integrate 4 fractional-N synthesizers that have the common reference frequency input. Wide list of attractive features and high level of customization make NT1066 capable to meet a demand of researchers and OEM developers in special applications: high precision positioning, goniometric, driverless car systems, professional drones and related areas.

2. FEATURES

Overall:

- 4 independent, fully customizable IQ channels
- 4 fractional-N PLLs with fully integrated VCOs and autotuning system
- Clock output for correlator with programmable frequency, amplitude and DC level
- Pass-through TCXO reference signal output
- Internal or external sampling frequency for 2-bit ADCs
- 4-wire SPI interface with user friendly registers map
- Individual status indicators of main subsystems (available in SPI registers) and cumulative status indicator (AOK, available both as a separate pin and in SPI registers)
- Embedded temperature sensor
- 12×12mm QFN108 package

Channels "A", "B" and "C" feature list:

- Single conversion super heterodyne architecture for L1, L2, L3, L5 bands of GNSS signals reception
- Active antenna detection system including short-protection circuit
- Tunable signal bandwidth up to 60MHz (up to 30MHz of IF BW with autocalibration system)
- IF AGC system or manually programmable gain
- Configurable output type: IQ or real with separate upper and lower sideband
- Analog differential output or 2-bit ADC digital output with programmable output logic high level

Channel "D" feature list:

- Direct conversion architecture with IQ data output for S band or L2, L3, L5 bands of GNSS signals reception or FM 65…110 MHz, VHF 160…240 MHz, UHF 470…862 MHz bands for DGPS data downloading
- Tunable signal bandwidth up to 20MHz (up to 10MHz of IF BW)
- Dual AGC system (RF + IF) or manually programmable gain
- Wide dynamic range with 1dB compression point up to +3 dBm @ S band
- Analog differential output with programmable thresholds or 2-bit ADC digital output with programmable output logic high level

3. DESCRIPTION

3.1. BLOCK DIAGRAM

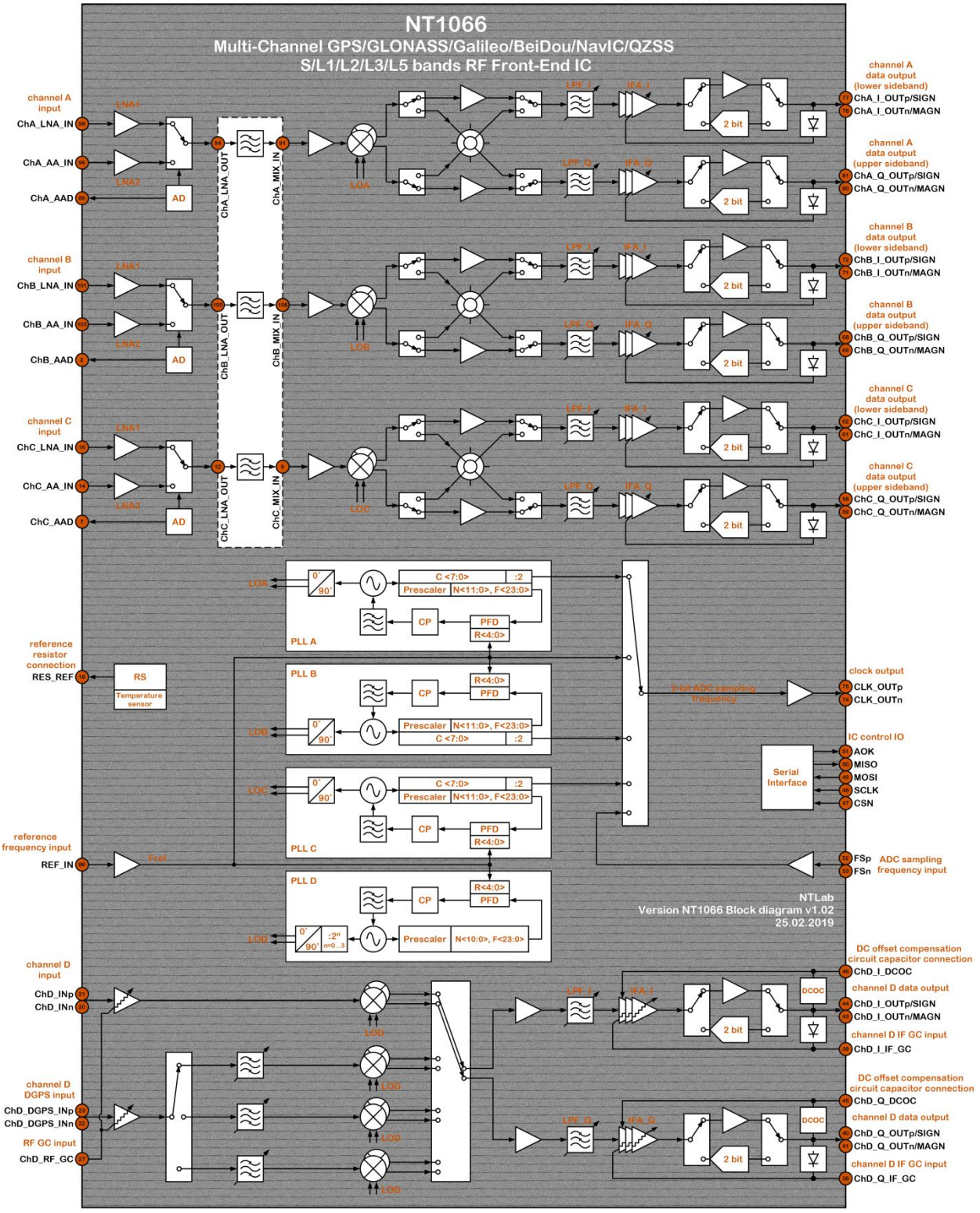


Figure 3.1: NT1066 Block diagram

3.2. APPLICATION SCHEMATIC

3.2.1. FULL APPLICATION SCHEMATIC

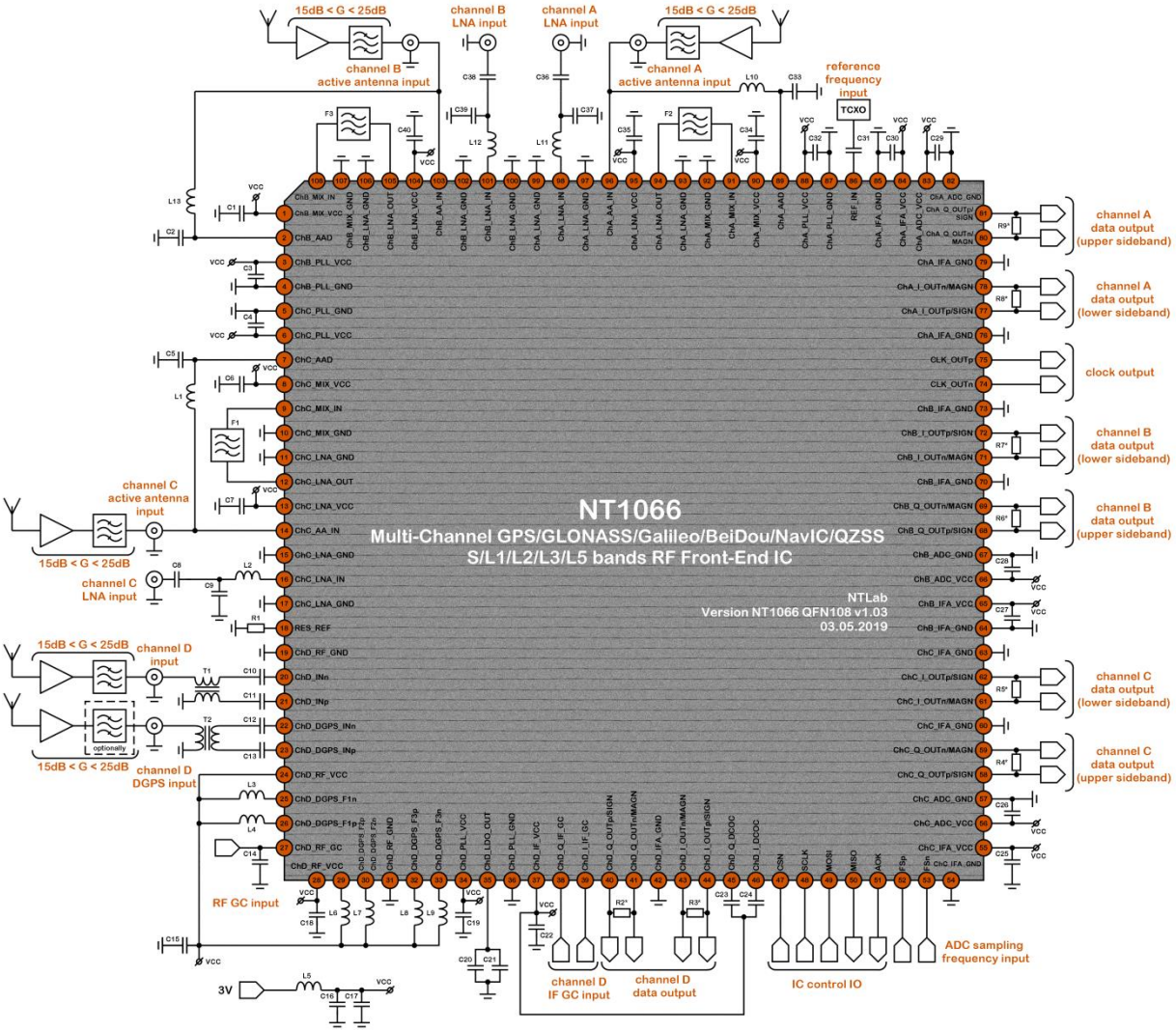


Figure 3.2: NT1066 Application schematic

Table 3.1: External component description

Component	Nominal value	Tolerance	Notes
C1	100nF	±10%	Supply voltage filtering capacitor
C2	1nF	±10%	Filtering capacitor
C3	100nF	±10%	Supply voltage filtering capacitor
C4	100nF	±10%	Supply voltage filtering capacitor
C5	1nF	±10%	Filtering capacitor
C6	100nF	±10%	Supply voltage filtering capacitor
C7	100nF	±10%	Supply voltage filtering capacitor
C8	18pF	±10%	DC blocking capacitor
C9[1]	1.2pF	±5%	Matching network capacitor for L1 band
	0.8pF	±5%	Matching network capacitor for L2, L3 and L5 bands
C10	100pF	±5%	Blocking capacitor
C11	100pF	±5%	Blocking capacitor
C12	220pF	±5%	Blocking capacitor
C13	220pF	±5%	Blocking capacitor
C14	10nF	±10%	Filtering capacitor
C15	100nF	±10%	Supply voltage filtering capacitor

Component	Nominal value	Tolerance	Notes
C16	10nF	±10%	Supply voltage filtering capacitor
C17	10µF	±10%	Supply voltage filtering capacitor
C18	100nF	±10%	Supply voltage filtering capacitor
C19	100nF	±10%	Supply voltage filtering capacitor
C20	1nF	±10%	Filtering capacitor
C21	100nF	±10%	Filtering capacitor
C22	100nF	±10%	Supply voltage filtering capacitor
C23	4.7µF	±10%	DCOC capacitor
C24	4.7µF	±10%	DCOC capacitor
C25	100nF	±10%	Supply voltage filtering capacitor
C26	100nF	±10%	Supply voltage filtering capacitor
C27	100nF	±10%	Supply voltage filtering capacitor
C28	100nF	±10%	Supply voltage filtering capacitor
C29	100nF	±10%	Supply voltage filtering capacitor
C30	100nF	±10%	Supply voltage filtering capacitor
C31	100pF	±10%	Blocking capacitor
C32	100nF	±10%	Supply voltage filtering capacitor
C33	1nF	±10%	Filtering capacitor
C34	100nF	±10%	Supply voltage filtering capacitor
C35	100nF	±10%	Supply voltage filtering capacitor
C36	18pF	±10%	DC blocking capacitor
C37[1]	1.2pF	±5%	Matching network capacitor for L1 band
	0.8pF	±5%	Matching network capacitor for L2, L3 and L5 bands
C38	18pF	±10%	DC blocking capacitor
C39[1]	1.2pF	±5%	Matching network capacitor for L1 band
	0.8pF	±5%	Matching network capacitor for L2, L3 and L5 bands
C40	100nF	±10%	Supply voltage filtering capacitor
L1	56nH (Q≥40)	±5%	AC blocking inductor
L2[1]	7.5nH	±5%	Matching network inductor for L1 band
	11nH	±5%	Matching network inductor for L2, L3 and L5 bands
L3	180nH (Q≥40)	±5%	Tracking filter inductor
L4	180nH (Q≥40)	±5%	Tracking filter inductor
L5	120Ohm / 100MHz	±20%	Supply voltage filtering inductor
L6	10nH (Q≥40)	±5%	Tracking filter inductor
L7	10nH (Q≥40)	±5%	Tracking filter inductor
L8	82nH (Q≥40)	±5%	Tracking filter inductor
L9	82nH (Q≥40)	±5%	Tracking filter inductor
L10	56nH (Q≥40)	±5%	AC blocking inductor
L11[1]	7.5nH	±5%	Matching network inductor for L1 band
	11nH	±5%	Matching network inductor for L2, L3 and L5 bands
L12[1]	7.5nH	±5%	Matching network inductor for L1 band
	11nH	±5%	Matching network inductor for L2, L3 and L5 bands
L13	56nH (Q≥40)	±5%	AC blocking inductor
R1	61.9kOhm	±1%	High precision resistor
R2[1]	1.5kOhm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R3[1]	1.5kOhm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R4[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R5[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R6[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R7[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output

Component	Nominal value	Tolerance	Notes
R8[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
R9[1]	510Ohm	±5%	Load resistor if analog differential output
	–	–	DNP if 2-bit ADC output
F1, F2, F3[1]	TA1658A	–	SAW filter for L1 band
	TA0871A	–	SAW filter for L2 band
	TFS1278A	–	SAW filter for E6 band
	TA1104A	–	SAW filter for L2, L3 and L5 band
T1	TC1-1-43A	–	Transformer
T2	MABA-007681-CT2010	–	Transformer

Note 1: Defined depending on PCB construction and purpose.

3.2.2. SPECIFIC APPLICATION SCHEMATIC

- If active antenna detector is not used, the following facilitated application schematic can be used for channel "A" (see Figure 3.3 and Table 3.2). The same application schematic can be used for channels "B" and "C". The following components can be excluded from the application schematic: C33 and L10 for channel "A", C2 and L13 for channel "B", C5 and L1 for channel "C".

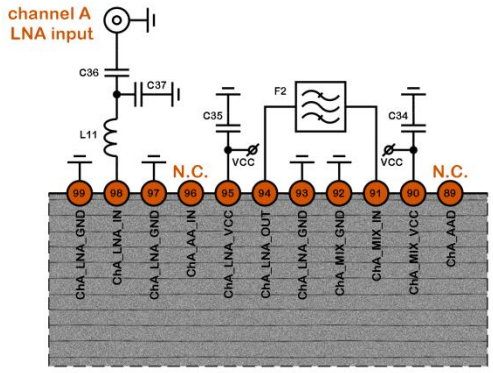


Figure 3.3: Channel "A" specific application schematic: active antenna detector is not used

Table 3.2: Channel "A" external components description

Component	Nominal value	
C34		100nF
C35		100nF
C36		18pF
C37	L1 band	1.2pF
	L2, L3, L5 bands	0.8pF
L11	L1 band	7.5nH
	L2, L3, L5 bands	11nH

- If channel "A", "B" or "C" is not used, the following facilitated application schematic can be used for disabled channel on the example of channel "A" (see Figure 3.4 and Table 3.3). The same application schematic can be used for channels "B" and "C". The following components can be excluded from the application schematic: C33, C36, C37, L10, L11, R8 and R9 for channel "A"; C2, C38, C39, L12, L13, R6 and R7 for channel "B"; C5, C8, C9, L1, L2, R4 and R5 for channel "C".

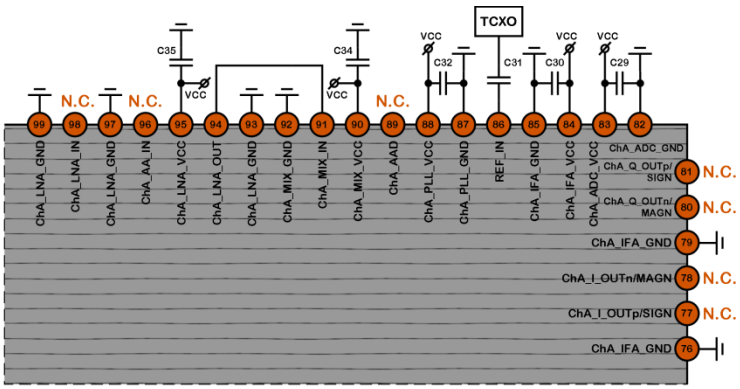


Figure 3.4: Channel "A" specific application schematic: channel is not used

Table 3.3: Channel "A" external components description

Component	Nominal value
C29	100nF
C30	100nF
C31	100pF
C32	100nF
C34	100nF
C35	100nF

- If channel “D” is not used, the following facilitated application schematic can be used (see Figure 3.5 and Table 3.4). Components C10–C14, L3–L4, L6–L9 and T1–T2 can be excluded from the application schematic.

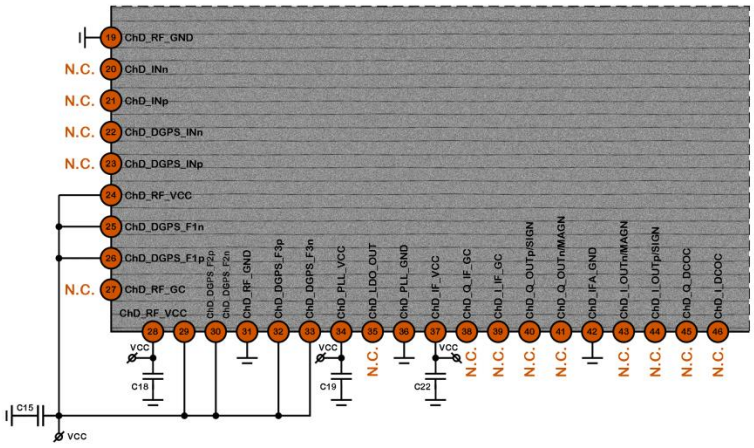


Figure 3.5: Channel “D” specific application schematic

Table 3.4: Channel “D” external components description

Component	Nominal value
C15	100nF
C18	100nF
C19	100nF
C22	100nF

- If navigational input of channel “D”, intended for L or S band receiving, is not used, the following facilitated application schematic can be used for channel “D” (see Figure 3.6 and Table 3.5). Components C10–C11 and T1 can be excluded from the application schematic.

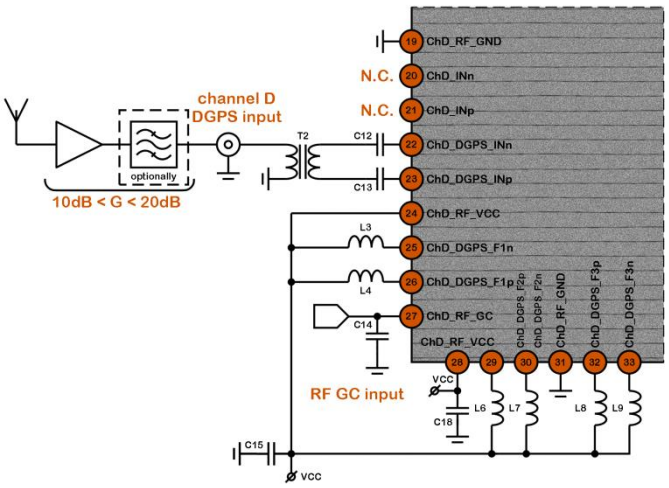


Figure 3.6: Channel “D” specific application schematic: ChD_INn and ChD_INp are not used

Table 3.5: Channel “D” external components description

Component	Nominal value
C12	220pF
C13	220pF
C14	10nF
C15	100nF
C18	100nF
L3	180nH (Q≥40)
L4	180nH (Q≥40)
L6	10nH (Q≥40)
L7	10nH (Q≥40)
L8	82nH (Q≥40)
L9	82nH (Q≥40)
T2	MABA-007681-CT2010

- If DGPS input of channel “D”, intended for FM, VHF or UHF band receiving, is not used, the following facilitated application schematic can be used for channel “D” (see Figure 3.7 and Table 3.6). Components C12–C13, L3–L4, L6–L9 and T2 can be excluded from the application schematic.

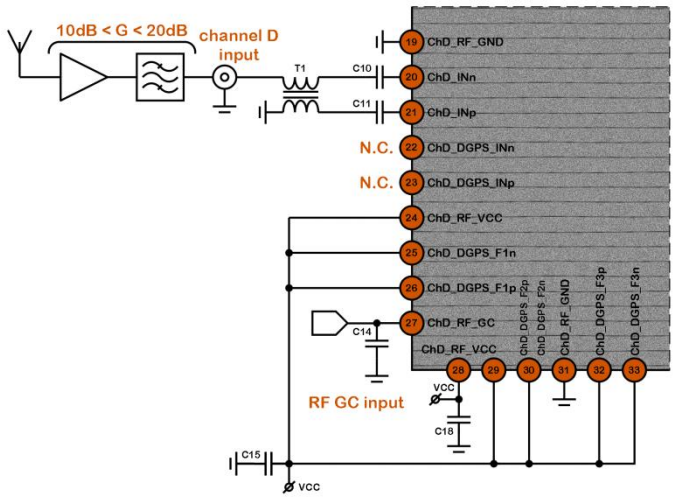


Figure 3.7: Channel “D” specific application schematic: ChD_DGPS_INn and ChD_DGPS_INp are not used

Table 3.6: Channel “D” external components description

Component	Nominal value
C10	100pF
C11	100pF
C14	10nF
C15	100nF
C18	100nF
T1	TC1-1-43A

3.3. PINS DESCRIPTION

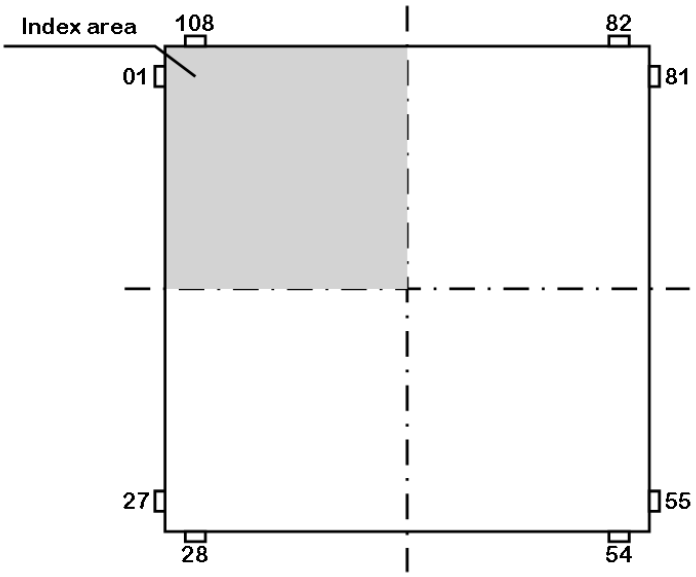


Figure 3.8: Pins configuration

Table 3.7: NT1066 pins description

#	Name	Description
1	ChB_MIX_VCC	Channel “B” mixer supply voltage
2	ChB_AAD	Channel “B” active antenna supply voltage output
3	ChB_PLL_VCC	Channel “B” PLL supply voltage
4	ChB_PLL_GND	Channel “B” PLL ground
5	ChC_PLL_GND	Channel “C” PLL ground
6	ChC_PLL_VCC	Channel “C” PLL supply voltage
7	ChC_AAD	Channel “C” active antenna supply voltage output
8	ChC_MIX_VCC	Channel “C” mixer supply voltage
9	ChC_MIX_IN	Channel “C” mixer input
10	ChC_MIX_GND	Channel “C” mixer ground
11	ChC_LNA_GND	Channel “C” LNA ground
12	ChC_LNA_OUT	Channel “C” LNA output
13	ChC_LNA_VCC	Channel “C” LNA supply voltage
14	ChC_AA_IN	Channel “C” active antenna input
15	ChC_LNA_GND	Channel “C” LNA ground
16	ChC_LNA_IN	Channel “C” LNA input
17	ChC_LNA_GND	Channel “C” LNA ground
18	RES_REF	External resistor for reference current source
19	ChD_RF_GND	Channel “D” RF ground
20	ChD_INn	Channel “D” analog input – complement
21	ChD_INp	Channel “D” analog input – true
22	ChD_DGPS_INn	Channel “D” DGPS analog input – complement
23	ChD_DGPS_INp	Channel “D” DGPS analog input – true
24	ChD_RF_VCC	Channel “D” RF circuits supply voltage
25	ChD_DGPS_F1n	Channel “D” FM tracking filter #1 load
26	ChD_DGPS_F1p	
27	ChD _RF_GC	Channel “D” RF external gain control input

#	Name	Description
28	ChD_RF_VCC	Channel “D” RF circuits supply voltage
29	ChD_DGPS_F2p	Channel “D” UHF tracking filter #2 load
30	ChD_DGPS_F2n	
31	ChD_RF_GND	Channel “D” RF ground
32	ChD_DGPS_F3p	Channel “D” VHF tracking filter #3 load
33	ChD_DGPS_F3n	
34	ChD_PLL_VCC	Channel “D” PLL supply voltage
35	ChD_LDO_OUT	Channel “D” LDO output
36	ChD_PLL_GND	Channel “D” PLL ground
37	ChD_IF_VCC	Channel “D” IF supply voltage
38	ChD_Q_IF_GC	Channel “D_Q” IF external gain control input
39	ChD_I_IF_GC	Channel “D_I” IF external gain control input
40	ChD_Q_OUTp/SIGN	Channel “D_Q” analog output – true; 2-bit ADC digital output data – SIGN
41	ChD_Q_OUTn/MAGN	Channel “D_Q” analog output – complement; 2-bit ADC digital output data – MAGN
42	ChD_IFA_GND	Channel “D” IFA ground
43	ChD_I_OUTn/MAGN	Channel “D_I” analog output – complement; 2-bit ADC digital output data – MAGN
44	ChD_I_OUTp/SIGN	Channel “D_I” analog output – true; 2-bit ADC digital output data – SIGN
45	ChD_Q_DCOC	Channel “D_Q” DC offset compensation circuit capacitor connection
46	ChD_I_DCOC	Channel “D_I” DC offset compensation circuit capacitor connection
47	CSN	SPI chip select
48	SCLK	SPI clock input
49	MOSI	SPI data input
50	MISO	SPI data output
51	AOK	Cumulative status indicator: “1” valid “0” fail
52	FSp	ADC sampling frequency analog input – true; LVDS input – positive; CMOS input
53	FSn	ADC sampling frequency analog input – complement; LVDS input – negative
54	ChC_IFA_GND	Channel “C” IFA ground
55	ChC_IFA_VCC	Channel “C” IFA supply voltage
56	ChC_ADC_VCC	Channel “C” ADC supply voltage
57	ChC_ADC_GND	Channel “C” ADC ground
58	ChC_Q_OUTp/SIGN	Channel “C_Q” analog output – true; 2-bit ADC digital output data – SIGN
59	ChC_Q_OUTn/MAGN	Channel “C_Q” analog output – complement; 2-bit ADC digital output data – MAGN
60	ChC_IFA_GND	Channel “C” IFA ground

#	Name	Description
61	ChC_I_OUTn/MAGN	Channel “C_I” analog output – complement; 2-bit ADC digital output data – MAGN
62	ChC_I_OUTp/SIGN	Channel “C_I” analog output – true; 2-bit ADC digital output data – SIGN
63	ChC_IFA_GND	Channel “C” IFA ground
64	ChB_IFA_GND	Channel “B” IFA ground
65	ChB_IFA_VCC	Channel “B” IFA supply voltage
66	ChB_ADC_VCC	Channel “B” ADC supply voltage
67	ChB_ADC_GND	Channel “B” ADC ground
68	ChB_Q_OUTp/SIGN	Channel “B_Q” analog output – true; 2-bit ADC digital output data – SIGN
69	ChB_Q_OUTn/MAGN	Channel “B_Q” analog output – complement; 2-bit ADC digital output data – MAGN
70	ChB_IFA_GND	Channel “B” IFA ground
71	ChB_I_OUTn/MAGN	Channel “B_I” analog output – complement; 2-bit ADC digital output data – MAGN
72	ChB_I_OUTp/SIGN	Channel “B_I” analog output – true; 2-bit ADC digital output data – SIGN
73	ChB_IFA_GND	Channel “B” IFA ground
74	CLK_OUTn	Clock frequency analog output – complement; LVDS output – negative
75	CLK_OUTp	Clock frequency analog output – true; LVDS output – positive; CMOS output
76	ChA_IFA_GND	Channel “A” IFA ground
77	ChA_I_OUTp/SIGN	Channel “A_I” analog output – true; 2-bit ADC digital output data – SIGN
78	ChA_I_OUTn/MAGN	Channel “A_I” analog output – complement; 2-bit ADC digital output data – MAGN
79	ChA_IFA_GND	Channel “A” IFA ground
80	ChA_Q_OUTn/MAGN	Channel “A_Q” analog output – complement; 2-bit ADC digital output data – MAGN
81	ChA_Q_OUTp/SIGN	Channel “A_Q” analog output – true; 2-bit ADC digital output data – SIGN
82	ChA_ADC_GND	Channel “A” ADC ground
83	ChA_ADC_VCC	Channel “A” ADC supply voltage
84	ChA_IFA_VCC	Channel “A” IFA supply voltage
85	ChA_IFA_GND	Channel “A” IFA ground
86	REF_IN	Reference frequency (TCXO) input
87	ChA_PLL_GND	Channel “A” PLL ground
88	ChA_PLL_VCC	Channel “A” PLL supply voltage
89	ChA_AAD	Channel “A” active antenna supply voltage output
90	ChA_MIX_VCC	Channel “A” mixer supply voltage
91	ChA_MIX_IN	Channel “A” mixer input
92	ChA_MIX_GND	Channel “A” mixer ground
93	ChA_LNA_GND	Channel “A” LNA ground
94	ChA_LNA_OUT	Channel “A” LNA output
95	ChA_LNA_VCC	Channel “A” LNA supply voltage

#	Name	Description
96	ChA_AA_IN	Channel “A” active antenna input
97	ChA_LNA_GND	Channel “A” LNA ground
98	ChA_LNA_IN	Channel “A” LNA input
99	ChA_LNA_GND	Channel “A” LNA ground
100	ChB_LNA_GND	Channel “B” LNA ground
101	ChB_LNA_IN	Channel “B” LNA input
102	ChB_LNA_GND	Channel “B” LNA ground
103	ChB_AA_IN	Channel “B” active antenna input
104	ChB_LNA_VCC	Channel “B” LNA supply voltage
105	ChB_LNA_OUT	Channel “B” LNA output
106	ChB_LNA_GND	Channel “B” LNA ground
107	ChB_MIX_GND	Channel “B” mixer ground
108	ChB_MIX_IN	Channel “B” mixer input

3.4. SERIAL INTERFACE DESCRIPTION

3.4.1. PROTOCOL DESCRIPTION

NT1066 can be configured with standard 4-wire SPI. In addition special pin “AOK” (low level interrupt) for unexpected system failure tracking is available.
User register map is split up into five parts according to functionality:

- system info;
- general settings and status;
- CLK settings;
- channels “A”, “B” and “C” settings and status (separate for each channel);
- channel “D” settings and status.

Available settings and status are listed in subsection 3.4.2.

3.4.1.1. GENERAL DESCRIPTION

Serial interface is used to read and change NT1066 data register information. It is intended for status monitoring, mode configuration and parameter adjustment.
Serial interface uses 4 pins for communication:

- CSN (serial interface chip select signal with low active level);
- MISO (serial interface output data);
- MOSI (serial interface input data);
- SCLK (serial interface clock).

Serial interface structure is shown on Figure 3.9.

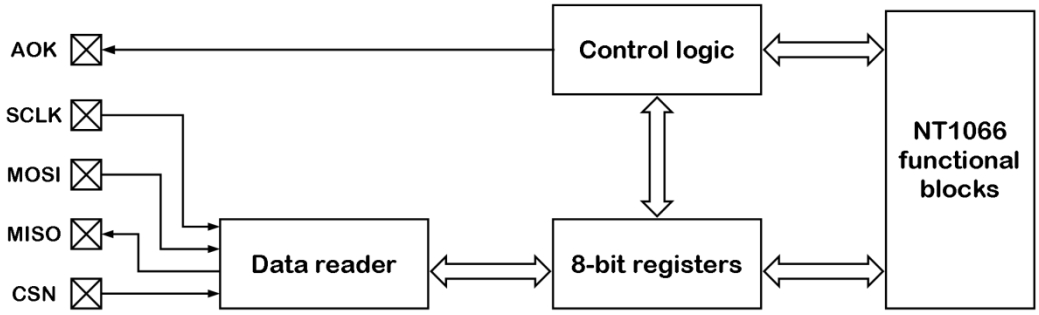


Figure 3.9: Serial interface structure

Data reader is intended for data exchange between 8-bit registers and external control unit using 4-wire serial bus. Data reader takes or changes values of internal trigger cells in the block of 8-bit registers. Internal trigger cells control internal blocks of NT1066 directly or through some logic elements.
Standard information packet (command) consists of three bytes and includes read/write attribute, AINC attribute, 14-bit address and 8-bit data. The first bit of a command is a read/write attribute: read operation is defined by “1” and write operation is defined by “0”. The second bit of a command is AINC attribute (data address automatic increment attribute), which automatically increases register address by “1”. A13…A0 bits represent address of the register to be read or written. D7…D0 bits are data to be read or written to the given address.
Communication is initialized by setting CSN to “0”. SCLK must be low at the beginning of any data transfer (falling CSN edge). Data format is always a bit sequence from first MSB to last LSB. All data transfers are framed by CSN signal, which must be low for any data transfer. In “idle” state, when CSN is high, SCLK, MOSI and MISO pins are blocked and don’t respond to external signals.

3.4.1.2. INFORMATION WRITING TO THE REGISTER

Single register writing is shown on Figure 3.10. Read/write attribute is set to “0” for writing mode. AINC attribute is set to “0”. Data is sampled into the NT1066 through the MOSI pin on the rising edges of SCLK. After CSN is set to “0”, first 16 bits of the command (write attribute, AINC attribute and register address) will be written to the interface on the 16 rising edges of SCLK. On the next 8 rising edges of SCLK D<7:0> data will be received. After that any rising edge of SCLK will be ignored. D<7:0> data will be written to the known address A<13:0> after last falling edge of SCLK.

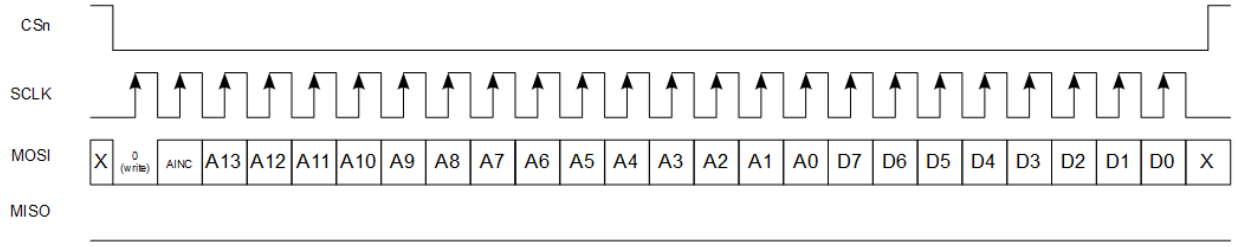


Figure 3.10: Single register writing

3.4.1.3. INFORMATION READING FROM THE REGISTER

Single register reading is shown on Figure 3.11. Read/write attribute is set to “1” for reading mode. AINC attribute is set to “0”. Data is sampled out of the NT1066 through the MISO pin on the falling edges of SCLK. After CSN is set to “0”, first 16 bits of the command (read attribute, AINC attribute and register address) will be written to the interface on the 16 rising edges of SCLK. On the next 8 falling edges of SCLK D<7:0> data from the register with A<13:0> address will send to MISO pin. D<7:0> data can be sampled by external control unit on the rising edge of SCLK. After data byte receiving CSN goes high, disabling the interface.

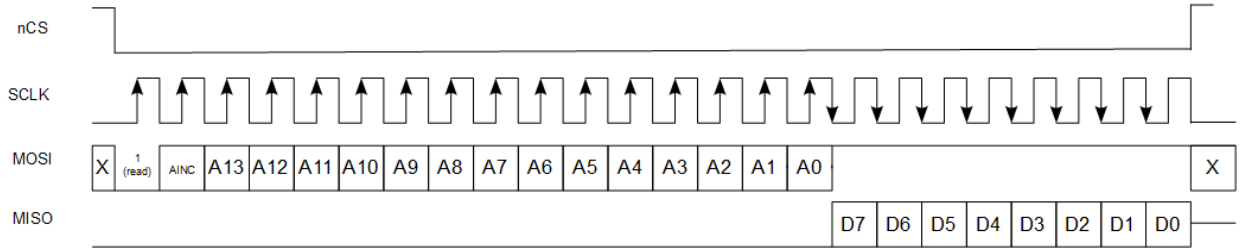


Figure 3.11: Single register reading

3.4.1.4. BURST DATA TRANSFER

NT1066 has a SPI burst-mode data transfer. AINC attribute should be set to “1” in order to automatically increment registers address. Unlike single data transfer CSN should be still “0” after LSB of the first data byte. CSN goes high to stop burst data transfer after the LSB of the last data byte.

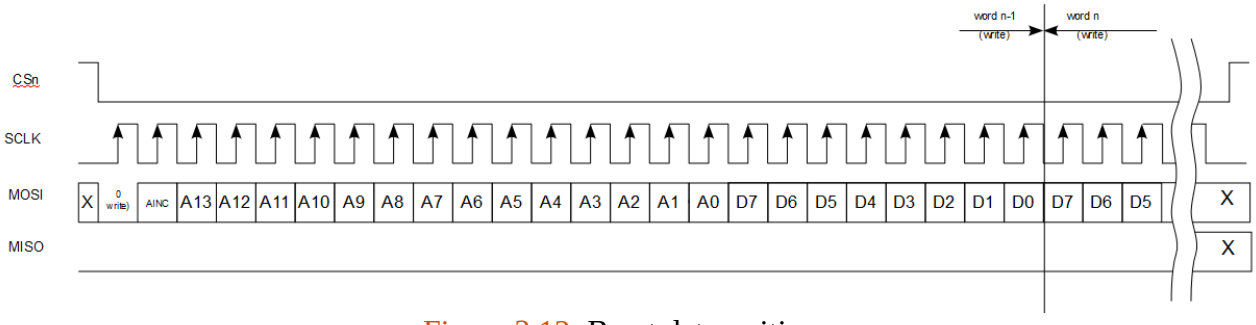


Figure 3.12: Burst data writing

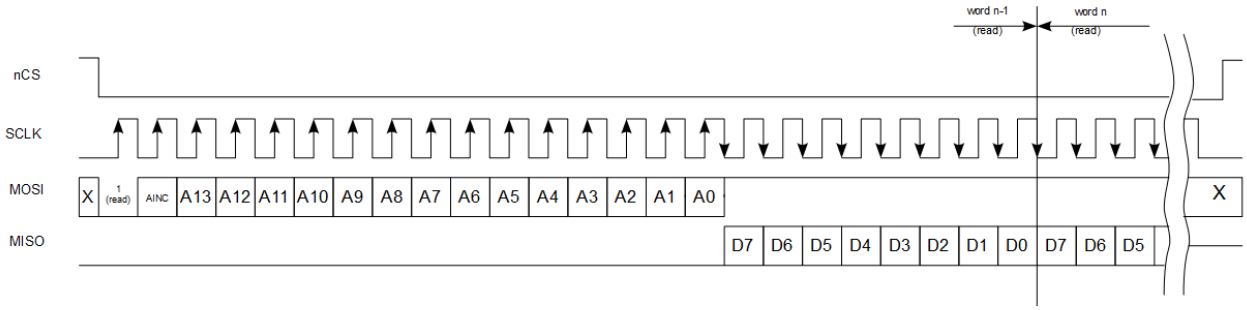


Figure 3.13: Burst data reading

3.4.1.5. TIMING DIAGRAM

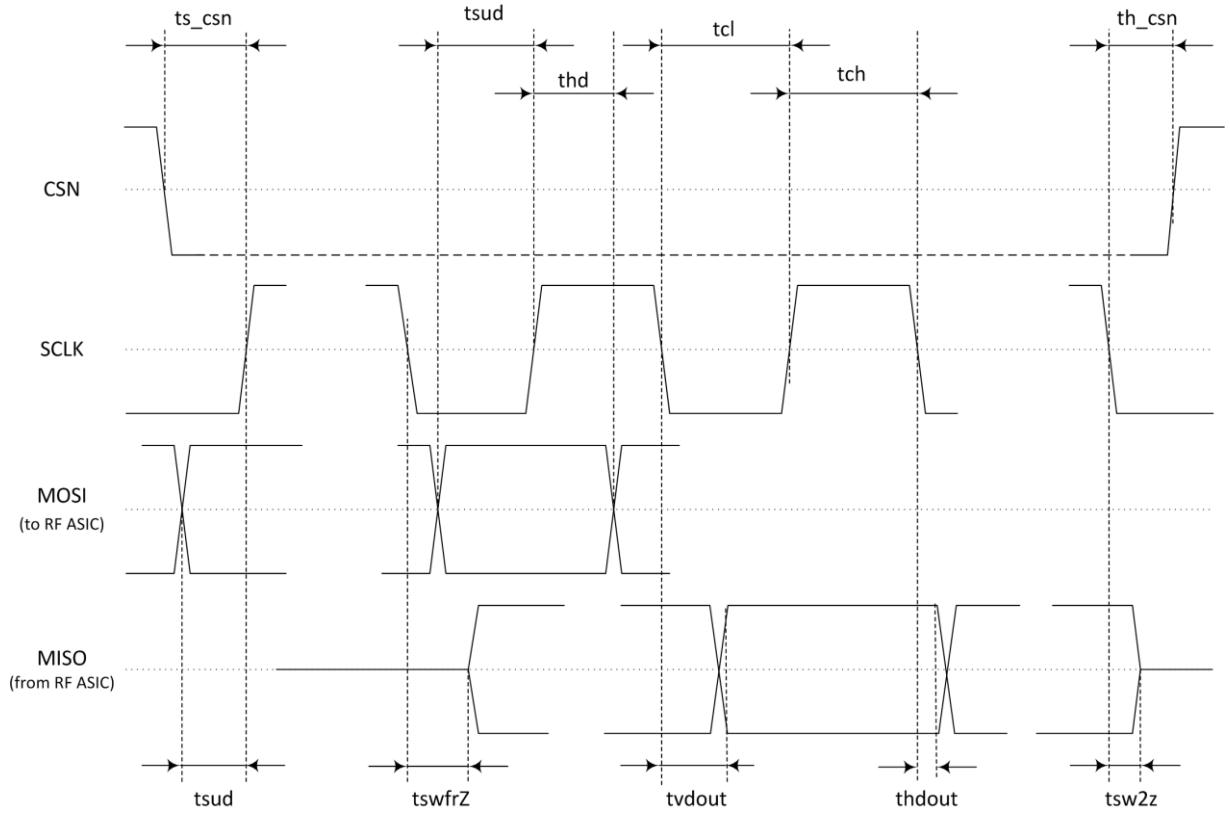


Figure 3.14: SPI timing diagram

Table 3.8: SPI timing

Parameter description	Symbol	Condition	Value			Unit
			min	typ.	max	
SCLK frequency	fclk	–	–	–	40	MHz
SCLK high and low time	tch tcl	1/fclk = (tch+tcl)	8	–	12	ns
Duty cycle	D	–	40	–	60	%
CSN setup time before SCLK	ts_csn	–	8	–	–	ns
CSN hold time	th_csn	–	4	–	–	ns
Data set up time	tsud	–	10	–	–	ns
Data hold time	thd	–	3	–	–	ns
Switch from Z-state time	tswfrZ	Load 20 pF	–	–	10	ns
Output data hold time	thdout	Load 20 pF	2.8	–	–	ns
Output data valid time	tvdout	Load 20 pF	–	–	10	ns
Switch to Z-state time	tsw2z	Load 20 pF	3	–	8	ns

3.4.2. PROGRAMMABLE REGISTERS

3.4.2.1. SYSTEM INFO

– Chip serial number, release

Bit number	Description	Default
Reg0, 0x00		
D7–D0 (MSB)	Chip serial number. $(0010000101010)_{dec}$ = 1066	"00100001"
Reg1, 0x01		
D7–D3 (LSB)	Continue. Refer to Reg0<D7–D0>.	"01010"
D2–D0	Chip version. $(010)_{dec}$ = 2 or $(011)_{dec}$ = 3	"010" or "011"

3.4.2.2. GENERAL SETTINGS AND STATUS

– General status (common AOK, channel "A" AOK, channel "B" AOK, channel "C" AOK, channel "D" AOK, die temperature)
– Common AOK indicator configuration (4 bits)
– Operation mode (channel "A" enable, channel "B" enable, channel "C" enable, channel "D" enable, CLK output enable)
– Reference frequency (value in kHz) //valid range is 10–50MHz
– Temperature measurement mode (single, continuous)
– Temperature measurement system execute

Bit number	Description	Default
Reg2, 0x02		
D7–D5	Unused	"000"
D4	Common cumulative status indicator: "0" fail "1" valid	–
D3	Channel "A" cumulative status indicator: "0" fail "1" valid	–
D2	Channel "B" cumulative status indicator: "0" fail "1" valid	–
D1	Channel "C" cumulative status indicator: "0" fail "1" valid	–
D0	Channel "D" cumulative status indicator: "0" fail "1" valid	–
Reg3, 0x03		
D7–D4	Unused	"0000"
D3	Channel "A" cumulative status as common AOK's component: "0" forbidden "1" permitted	"1"
D2	Channel "B" cumulative status as common AOK's component: "0" forbidden "1" permitted	"1"
D1	Channel "C" cumulative status as common AOK's component: "0" forbidden "1" permitted	"1"

Bit number	Description	Default
D0	Channel “D” cumulative status as common AOK’s component: “0” forbidden “1” permitted	“1”
Reg4, 0x04		
D7–D2	Unused	“000000”
D1–D0 (MSB)	Temperature sensor indicator: T = 506 – 0.755× (Reg4<D1–D0>$_{dec}$ + Reg5<D7–D0>$_{dec}$) “0000000000” not valid range … … “1000011000” not valid range “1000011001” +100 °C “1001111101” 25 “1011010011” –40 °C “1011010100” not valid range … … “1111111111” not valid range	–
Reg5, 0x05		
D7–D0 (LSB)	Continue. Refer to Reg4<D1–D0>.	–
Reg6, 0x06		
D7–D5	Unused	“000”
D4	Clock output enable: “0” disabled “1” enabled	“0”
D3	Channel “D” enable: “0” disabled “1” enabled	“0”
D2	Channel “C” enable: “0” disabled “1” enabled	“0”
D1	Channel “B” enable: “0” disabled “1” enabled	“0”
D0	Channel “A” enable: “0” disabled “1” enabled	“0”
Reg7, 0x07		
D7–D0 (MSB)	Reference oscillator frequency, kHz. ***Note:*** *Valid range is 10–50MHz.*	“00100111”
Reg8, 0x08		
D7–D0 (LSB)	Continue. Refer to Reg7<D7–D0>.	“00010000”
Reg9, 0x09		
D7–D2	Unused	“000000”
D1	Temperature measurement mode: “0” single “1” continuous	“0”
D0	Temperature measurement system execution: “0” finished “1” start (automatically reset to “0” when finished)	“0”

3.4.2.3. CLK SETTINGS

- CLK frequency and ADC sampling frequency source (PLL “A”, PLL “B”, PLL “C”, external via pins #52–53, reference frequency pass-through)
- C-divider ratio (:4, :5 … :255) //if PLL “A”, PLL “B”, PLL “C” CLK frequency source
- CLK output type (CMOS, ECL, LVDS)
- CLK amplitude //2 bits if ‘ECL’ type; 2 bits if ‘LVDS’ type
- CLK output DC level (2 bits) //if ‘ECL’ type
- CLK output voltage (3 bits) //if ‘CMOS’ type
- Sampling frequency input type (LVDS, ECL/CMOS)
- Internal terminator enable //if ‘LVDS’ type
- Internal terminator value (2 bits) //if ‘LVDS’ type

Bit number	Description	Default
Reg10, 0x0A		
D7–D5	Unused	“000”
D4–D3	Clock output type: “00” CMOS (recommended for F_{CLK} up to 100MHz) “01” ECL (not recommended for use) “10” LVDS (recommended for F_{CLK} up to 120MHz) “11” high resistance state	“10”
D2–D0	Clock frequency and ADC sampling frequency source: “000” PLL “A” “001” PLL “B” “010” PLL “C” “011” reference frequency pass-through “100” external sampling frequency via pins #52–53	“000”
Reg11, 0x0B		
D7–D0	Clock C-divider ratio (refer to formula in section 6.11 for F_{CLK} calculation): “00000100” 4 ... with step of 1 “11111111” 255 ***Note:*** *Available if clock frequency and ADC sampling frequency source is PLL “A”, “B” or “C” (if Reg10<D2–D0> = “000”, “001”, “010”).*	“00010110”
Reg12, 0x0C		
D7	Unused	“0”
D6–D5	Clock amplitude (V_{CLK}): LVDS ECL “00” 290 mVp-p 420 mVp-p “01” 450 mVp-p 550 mVp-p “10” 600 mVp-p 690 mVp-p “11” 760 mVp-p 770 mVp-p	“01”
D4–D3	Clock output DC level (V_{OH_CLK}, V): “00” 1.8 – 0.25×Reg12<D6–D5> “01” 1.95 – 0.25×Reg12<D6–D5> “10” 2.7 – 0.25×Reg12<D6–D5> “11” 2.85 – 0.25×Reg12<D6–D5> ***Note:*** *Available if clock output type is ECL (if Reg10<D4–D3> = “01”).*	“11”
D2–D0	Clock output logic-level high: “000” 1.8 V “001” 1.95 V “010” 2.7 V “011” 2.85 V “1XX” VCC – 0.1V ***Note:*** *Available if clock output type is CMOS (if Reg10<D4–D3> = “00”).*	“011”

Bit number	Description	Default
Reg13, 0x0D		
D7–D4	Unused	"0000"
D3–D2	Internal terminator value: "00" 90 Ohm "01" 100 Ohm "10" 100 Ohm "11" 110 Ohm	"01"
	Note: *If external sampling frequency input type is LVDS (if Reg13<D0> = "1").*	
D1	Internal terminator enable: "0" disabled "1" enabled	"0"
	Note: *If external sampling frequency input type is LVDS (if Reg13<D0> = "1").*	
D0	External sampling frequency input type: "0" ECL/CMOS "1" LVDS	"1"

3.4.2.4. CHANNELS "A", "B", "C" SETTINGS AND STATUS

- Channel status (channel AOK, LNA status, active antenna indicators, PLL lock indicator, VCO voltage comparator status, LPF autocalibration system status)
- Channel AOK configuration (active antenna current indicator, PLL lock indicator, VCO voltage comparator status, LPF autocalibration system status, tuning systems status)
- Channel mode (IQ, upper sideband, lower sideband, lower sideband + upper sideband)
- LO frequency (value in kHz) //valid range is 1550–1615MHz if L1 band; 1160–1300MHz if L2, L3, L5 bands
- PLL mode (integer-N, fractional-N)
- R-divider ratio (:1, :2 … :31) //if 'integer-N' PLL mode
- N-divider ratio (:16, :17 … :4095) //if 'integer-N' PLL mode
- PLL tuning system execute
- IF I passband (7 bits) //if IQ, lower + upper sidebands or lower sideband
- IF Q passband (7 bits) //if IQ, lower + upper sidebands or upper sideband
- LPF autocalibration system execute
- IF GC mode (automatic, manual via SPI)
- IF I gain (10 bits) //if manual GC mode
- IF Q gain (10 bits) //if manual GC mode
- Output data interface (analog differential output, 2-bit ADC output)
- IF AGC thresholds (7 bits) //if 2-bit ADC output and automatic IF GC mode
- 2-bit ADC logic-level high (1.8V, 2.0V, 2.5V, VCC)
- 2-bit ADC type (clocked by rising edge, clocked by falling edge, asynchronous)

Bit number	Description	Default
Reg14, 0x0E for Channel "A" / Reg36, 0x24 for Channel "B" / Reg58, 0x3A for Channel "C"		
D7	Channel# LNA1 enable status	–
D6	Channel# LNA2 enable status	–
D5	Channel# PLL status: "0" not locked "1" locked	–
D4–D3	Channel# VCO voltage comparator status: "00" valid "01" upper threshold exceeded (oscillation frequency is too high) "10" lower threshold exceeded (oscillation frequency is too low) "11" unused	–
D2	Channel# active antenna connection indicator: "0" not connected (active antenna current is too low) "1" connected (active antenna current is within limits) ***Note:*** *Available if active antenna detector is enabled (if Reg34<D2> for Channel "A" / Reg56<D2> for Channel "B" / Reg78<D2> for Channel "C" is "1").*	–
D1	Channel# active antenna current indicator: "0" valid (active antenna current is within or below limits) "1" upper threshold exceeded (active antenna current is too high) ***Note:*** *Available if active antenna detector is enabled (if Reg34<D2> for Channel "A" / Reg56<D2> for Channel "B" / Reg78<D2> for Channel "C" is "1").*	–
D0	Channel# LPF autocalibration system status: "0" error "1" completed successfully	–
Reg15, 0x0F for Channel "A" / Reg37, 0x25 for Channel "B" / Reg59, 0x3B for Channel "C"		
D7–D5	Unused	"000"
D4	Channel# PLL status as channel AOK's component: "0" forbidden "1" permitted	"1"
D3	Channel# VCO voltage comparator status as channel AOK's component: "0" forbidden "1" permitted	"1"
D2	Channel# tuning systems status as channel AOK's component: "0" forbidden "1" permitted	"1"
D1	Channel# active antenna current indicator as channel AOK's component: "0" forbidden "1" permitted	"1"
D0	Channel# LPF autocalibration system status as AOK's component: "0" forbidden "1" permitted	"1"
Reg16, 0x10 for Channel "A" / Reg38, 0x26 for Channel "B" / Reg60, 0x3C for Channel "C"		
D7–D2	Unused	"000000"
D1–D0	Channel# mode: "00" Channel I: IQ mode disabled; Channel Q: IQ mode upper sideband "01" Channel I: lower sideband; Channel Q: disabled "10" Channel I: lower sideband; Channel Q: upper sideband	"00"

Bit number	Description	Default
Reg17, 0x11 for Channel "A" / Reg39, 0x27 for Channel "B" / Reg61, 0x3D for Channel "C"		
D7	Unused	"0"
D6–D0 (MSB)	Channel# LO frequency, kHz.	Ch "A" "0011000" Ch "B" "0010010" Ch "C" "0010010"
Reg18, 0x12 for Channel "A" / Reg40, 0x28 for Channel "B" / Reg62, 0x3E for Channel "C"		
D7–D0	Continue. Refer to Reg17<D6–D0> for Channel "A" / Reg39<D6–D0> for Channel "B" / Reg61<D6–D0> for Channel "C".	Ch "A" "01000010" Ch "B" "11011000" Ch "C" "00101000"
Reg19, 0x13 for Channel "A" / Reg41, 0x29 for Channel "B" / Reg63, 0x3F for Channel "C"		
D7–D0 (LSB)	Continue. Refer to Reg17<D6–D0> for Channel "A" / Reg39<D6–D0> for Channel "B" / Reg61<D6–D0> for Channel "C".	Ch "A" "11110000" Ch "B" "00111000" Ch "C" "01110000"
Reg20, 0x14 for Channel "A" / Reg42, 0x2A for Channel "B" / Reg64, 0x40 for Channel "C"		
D7–D1	Unused	"0000000"
D0	Channel# PLL mode: "0" integer-N "1" fractional-N	"1"
Reg21, 0x15 for Channel "A" / Reg43, 0x2B for Channel "B" / Reg65, 0x41 for Channel "C"		
D7–D5	Unused	"000"
D4–D0	Channel# R-divider ratio (refer to formula in section 6.3 for F_{LO} calculation): "00000" unused "00001" 1 … with step of 1 "11111" 31 ***Note:*** *Available If PLL mode is integer-N (if Reg20<D0> for Channel "A" / Reg42<D0> for Channel "B" / Reg64<D0> for Channel "C" is "0").*	"00001"
Reg22, 0x16 for Channel "A" / Reg44, 0x2C for Channel "B" / Reg66, 0x42 for Channel "C"		
D7–D4	Unused	"0000"
D3–D0 (MSB)	Channel# N-divider ratio (refer to formula in section 6.3 for F_{LO} calculation): "000000000000" unused … unused "000000001111" unused "000000010000" 16 … with step of 1 "111111111111" 4095 ***Note:*** *Available If PLL mode is integer-N (if Reg20<D0> for Channel "A" / Reg42<D0> for Channel "B" / Reg64<D0> for Channel "C" is "0").*	Ch "A" "0001" Ch "B" "0000" Ch "C" "0000"
Reg23, 0x17 for Channel "A" / Reg45, 0x2D for Channel "B" / Reg67, 0x43 for Channel "C"		
D7–D0 (LSB)	Continue. Refer to Reg22<D3–D0> for Channel "A" / Reg44<D3–D0> for Channel "B" / Reg66<D3–D0> for Channel "C".	Ch "A" "00111110" Ch "B" "11110111" Ch "C" "11101110"

Bit number	Description	Default
Reg24, 0x18 for Channel "A" / Reg46, 0x2E for Channel "B" / Reg68, 0x44 for Channel "C"		
D7–D1	Unused	"0000000"
D0	Channel# PLL divider ratio calculation and subband autoselection system execution: "0" finished "1" start (reset to "0" automatically when finished)	"0"
Reg25, 0x19 for Channel "A" / Reg47, 0x2F for Channel "B" / Reg69, 0x45 for Channel "C"		
D7	Unused	"0"
D6–D0	Channel# LPF_I cut-off frequency: "0000000" 8.9 MHz not guaranteed range … "0010000" 13.0 MHz not guaranteed range "0010001" 13.3 MHz … "0011001" 15.3 MHz … "0101011" 19.6 MHz … "1000001" 24.6 MHz … "1011001" 29.7 MHz "1011010" 29.9 MHz not guaranteed range … "1111111" 37.1 MHz not guaranteed range ***Note:*** *Available if channel mode in Reg16<D1–D0> for Channel "A" / Reg38<D1–D0> for Channel "B" / Reg60<D1–D0> for Channel "C" is "00", "10", "11".*	Ch "A" "1011001" Ch "B" "0101011" Ch "C" "1011001"
Reg26, 0x1A for Channel "A" / Reg48, 0x30 for Channel "B" / Reg70, 0x46 for Channel "C"		
D7	Unused	"0"
D6–D0	Channel# LPF_Q cut-off frequency: "0000000" 8.9 MHz not guaranteed range … "0010000" 13.0 MHz not guaranteed range "0010001" 13.3 MHz … "0011001" 15.3 MHz … "0101011" 19.6 MHz … "1000001" 24.6 MHz … "1011001" 29.7 MHz "1011010" 29.9 MHz not guaranteed range … "1111111" 37.1 MHz not guaranteed range ***Note:*** *Available if channel mode in Reg16<D1–D0> for Channel "A" / Reg38<D1–D0> for Channel "B" / Reg60<D1–D0> for Channel "C" is "00", "01", "11".*	Ch "A" "1011001" Ch "B" "0101011" Ch "C" "1011001"
Reg27, 0x1B for Channel "A" / Reg49, 0x31 for Channel "B" / Reg71, 0x47 for Channel "C"		
D7–D1	Unused	"0000000"
D0	Channel# LPF autocalibration system execution: "0" finished "1" start (reset to "0" automatically when finished)	"0"
Reg28, 0x1C for Channel "A" / Reg50, 0x32 for Channel "B" / Reg72, 0x48 for Channel "C"		
D7–D6	Unused	"00"
D5–D4	Channel# 2-bit ADC type: "0X" asynchronous "10" clocked by falling edge "11" clocked by rising edge ***Note:*** *Available if output data interface is 2-bit ADC (if Reg28<D1–D0> for Channel "A" / Reg50<D1–D0> for Channel "B" / Reg72< D1–D0> for Channel "C" is "11").*	"10"

<table>
<tr><th>Bit number</th><th colspan="2">Description</th><th>Default</th></tr>
<tr><td>D3–D2</td><td colspan="2">Channel# 2-bit ADC logic-level high:
“00” 1.8V
“01” 2.0V
“10” 2.5V
“11” VCC
Note: Available if output data interface is 2-bit ADC (if Reg28<D1–D0> for Channel “A” / Reg50<D1–D0> for Channel “B” / Reg72<D1–D0> for Channel “C” is “11”).</td><td>“11”</td></tr>
<tr><td>D1</td><td colspan="2">Channel# IFA gain control mode:
“0” manual
“1” automatic</td><td>“1”</td></tr>
<tr><td>D0</td><td colspan="2">Channel# output data interface:
“0” analog differential
“1” 2-bit ADC</td><td>“1”</td></tr>
<tr><td colspan="4">Reg29, 0x1D for Channel “A” / Reg51, 0x33 for Channel “B” / Reg73, 0x49 for Channel “C”</td></tr>
<tr><td>D7–D2</td><td colspan="2">Unused</td><td>“000000”</td></tr>
<tr><td>D1–D0 (MSB)</td><td>Channel# IFA_I gain value:
“0000000000” 1.7 dB
… …
“0011101000” 2.2 dB
… …
“0011110111” 5.0 dB
… …
“0100001001” 10.1 dB
… …
“0100110000” 13.0 dB
… …
“0101001100” 18.1 dB
… …
“0101101001” 23.1 dB
… …
“0110100011” 27.1 dB
… …
“0110110101” 30.0 dB
… …
“0111000011” 33.1 dB
… …
“0111110000” 37.1 dB
… …
“1000011110” 41.1 dB
… …
“1001011000” 45.0 dB
… …
“1010010110” 48.1 dB
… …
“1010110001” 52.0 dB
… …
“1011101010” 56.0 dB
… …
“1011110100” 57.5 dB
… …
“1100011000” 59.0 dB
… …
“1111111111” 59.2 dB
Note: If Reg28<D1–D0> for Channel “A” / Reg50<D1–D0> for Channel “B” / Reg72<D1–D0> for Channel “C” is “10.</td><td>Channel# IFA_I digital detector threshold w.r.t. sinewave signal:
“0000000000” 0 %
… …
“0101000000” 30%
… …
“0111111111” 45%
… …
“1100110010” 73%
… …
“1111111111” 96%

Note: If Reg28<D1–D0> for Channel “A” / Reg50<D1–D0> for Channel “B” / Reg72<D1–D0> for Channel “C” is “11”.</td><td>“01”</td></tr>
</table>

<table>
<tr><th>Bit number</th><th colspan="2">Description</th><th>Default</th></tr>
<tr><td colspan="4">Reg30, 0x1E for Channel “A” / Reg52, 0x34 for Channel “B” / Reg74, 0x4A for Channel “C”</td></tr>
<tr><td>D7–D0
(LSB)</td><td colspan="2">Continue. Refer to Reg29<D1–D0> for Channel “A” / Reg51<D1–D0> for Channel “B” / Reg73<D1–D0> for Channel “C”.</td><td>“00101100”</td></tr>
<tr><td colspan="4">Reg31, 0x1F for Channel “A” / Reg53, 0x35 for Channel “B” / Reg75, 0x4B for Channel “C”</td></tr>
<tr><td>D7–D2</td><td colspan="2">Unused</td><td>“000000”</td></tr>
<tr><td rowspan="2">D1–D0
(MSB)</td><td>Channel# IFA_Q gain value:
“0000000000” 1.7 dB
… …
“0011101000” 2.2 dB
… …
“0011110111” 5.0 dB
… …
“0100001001” 10.1 dB
… …
“0100110000” 13.0 dB
… …
“0101001100” 18.1 dB
… …
“0101101001” 23.1 dB
… …
“0110100011” 27.1 dB
… …
“0110110101” 30.0 dB
… …
“0111000011” 33.1 dB
… …
“0111110000” 37.1 dB
… …
“1000011110” 41.1 dB
… …
“1001011000” 45.0 dB
… …
“1010010110” 48.1 dB
… …
“1010110001” 52.0 dB
… …
“1011101010” 56.0 dB
… …
“1011110100” 57.5 dB
… …
“1100011000” 59.0 dB
… …
“1111111111” 59.2 dB</td><td>Channel# IFA_Q digital detector threshold w.r.t. sinewave signal:
“0000000000” 0 %
… …
“0101000000” 30%
… …
“0111111111” 45%
… …
“1100110010” 73%
… …
“1111111111” 96%

Note: If Reg28<D1–D0> for Channel “A” / Reg50<D1–D0> for Channel “B” / Reg72<D1–D0> for Channel “C” is “11”.</td><td rowspan="2">“01”</td></tr>
<tr><td>Note: If Reg28<D1–D0> for Channel “A” / Reg50<D1–D0> for Channel “B” / Reg72<D1–D0> for Channel “C” is “10”.</td></tr>
<tr><td colspan="4">Reg32, 0x20 for Channel “A” / Reg54, 0x36 for Channel “B” / Reg76, 0x4C for Channel “C”</td></tr>
<tr><td>D7–D0
(LSB)</td><td colspan="2">Continue. Refer to Reg31<D1–D0> for Channel “A” / Reg53<D1–D0> for Channel “B” / Reg75<D1–D0> for Channel “C”.</td><td>“00101100”</td></tr>
</table>

Active antenna detection system:

- Active antenna detector enable
- Active antenna current (4 bits)
- AAD system behavior if short circuit detected (current limitation, minimum current restriction)
- LNA1/LNA2 switching mode (automatic, manual)
- LNA1/LNA2 enable //if manual switching mode

Bit number	Description	Default
Reg33, 0x21 for Channel "A" / Reg55, 0x37 for Channel "B" / Reg77, 0x4D for Channel "C"		
D7–D4	Channel# active antenna current consumption (typical): "0000" 2 mA "0001" 4 mA "0010" 6 mA "0011" 8 mA "0100" 10 mA "0101" 12 mA "0110" 14 mA "0111" 16 mA "1000" 18 mA "1001" 20 mA "1010" 22 mA "1011" 24 mA "1100" 26 mA "1101" 28 mA "1110" 30 mA "1111" 32 mA ***Note:*** *Available if active antenna detector is enabled (if Reg34<D2> for Channel "A" / Reg56<D2> for Channel "B" / Reg78<D2> for Channel "C" is "1").*	"0011"
D3–D1	Unused	"000"
D0	Channel# active antenna detector behavior if short circuit detected: "0" current limitation "1" minimum current restriction ***Note:*** *Available if active antenna detector is enabled (if Reg34<D2> for Channel "A" / Reg56<D2> for Channel "B" / Reg78<D2> for Channel "C" is "1").*	"0"
Reg34, 0x22 for Channel "A" / Reg56, 0x38 for Channel "B" / Reg78, 0x4E for Channel "C"		
D7–D4	Unused	"0000"
D3	Channel# active antenna detector permission for autoselection of LNA1 or LNA2: "0" forbidden "1" permitted ***Note:*** *Available if active antenna detector is enabled (if Reg34<D2> for Channel "A" / Reg56<D2> for Channel "B" / Reg78<D2> for Channel "C" is "1").*	"1"
D2	Channel# active antenna detector enable: "0" disabled "1" enabled	"1"
D1	Channel# LNA enable: "0" disabled "1" enabled ***Note:*** *Available if autoselection is forbidden (if Reg34<D3> for Channel "A" / Reg56<D3> for Channel "B" / Reg78<D3> for Channel "C" is "0").*	"1"
D0	Channel# LNA type: "0" LNA1 "1" LNA2 ***Note:*** *Available if autoselection is forbidden and LNA is enabled (if Reg34<D3> for Channel "A" / Reg56<D3> for Channel "B" / Reg78<D3> for Channel "C" is "0" and Reg34<D1> for Channel "A" / Reg56<D1> for Channel "B" / Reg78<D1> for Channel "C" is "1").*	"0"

Calibration and test section:

– IQ phase correction (6 bits)

Bit number	Description	Default
Reg35, 0x23 for Channel "A" / Reg57, 0x39 for Channel "B" / Reg79, 0x4F for Channel "C"		
D7–D6	Unused	"00"
D5–D0	Channel# IQ phase correction: "000000" 74.1° … … "011111" 89.8° "100000" 90° "100001" 90.3° … … "111111" 104.9°	"011111"

3.4.2.5. CHANNEL "D" SETTINGS AND STATUS

– Channel status (channel AOK, PLL lock indicator, VCO voltage comparator status, RF gain, IF gain)
– Channel AOK configuration (PLL lock indicator, VCO voltage comparator status, tuning systems status)
– LO frequency (value in KHz) //valid range is 2480–2500MHz if S band; 1170–1290MHz if L2, L3, L5 bands; 65–110MHz if FM band; 160–240MHz if VHF band; 470–862MHz if UHF band
– PLL tuning system execute
– RF GC mode (automatic, manual via SPI, external via pin #27)
– RF gain (4 bits) //if manual GC mode
– IF passband (8 bits)
– IF GC mode (automatic, manual via SPI, external via pins #38–39)
– IF I gain (9 bits) //if manual GC mode
– IF Q gain (9 bits) //if manual GC mode
– IFA output DC level (2 bits) //if 'analog differential' type
– Output data interface (analog differential output, 2-bit ADC output)
– IF AGC thresholds (7 bits)
– 2-bit ADC logic-level high (1.8V, 2.0V, 2.5V, VCC)
– 2-bit ADC type (asynchronous, clocked by rising edge, clocked by falling edge)

Bit number	Description	Default
Reg80, 0x50		
D7–D3	Unused	"00000"
D2–D1	Channel "D" VCO voltage comparator status: "00" valid "01" upper threshold exceeded (oscillation frequency is too high) "10" lower threshold exceeded (oscillation frequency is too low) "11" unused	–
D0	Channel "D" PLL status: "0" not locked "1" locked	–
Reg81, 0x51		
D7–D4	Unused	"0000"
D3–D0	Channel "D" RF gain status.	–

Bit number	Description	Default
Reg82, 0x52		
D7–D1	Unused	"0000000"
D0 (MSB)	Channel "D" IFA_I gain status.	–
Reg83, 0x53		
D7–D0 (LSB)	Continue. Refer to Reg82<D0>.	–
Reg84, 0x54		
D7–D1	Unused	"0000000"
D0 (MSB)	Channel "D" IFA_Q gain status.	–
Reg85, 0x55		
D7–D0 (LSB)	Continue. Refer to Reg84<D0>.	–
Reg86, 0x56		
D7–D3	Unused	"00000"
D2	Channel "D" PLL status as channel AOK's components: "0" forbidden "1" permitted	"1"
D1	Channel "D" VCO voltage comparator status as channel AOK's component: "0" forbidden "1" permitted	"1"
D0	Channel "D" tuning systems status as channel AOK's component: "0" forbidden "1" permitted	"1"
Reg87, 0x57		
D7	Unused	"0"
D6–D0 (MSB)	Channel "D" LO frequency, kHz.	"0100110"
Reg88, 0x58		
D7–D0	Continue. Refer to Reg87<D6–D0>.	"00000110"
Reg89, 0x59		
D7–D0 (LSB)	Continue. Refer to Reg87<D6–D0>.	"01100000"
Reg90, 0x5A		
D7–D1	Unused	"0000000"
D0	Channel "D" PLL divider ratio calculation and subband autoselection system execution: "0" finished "1" start (reset to "0" automatically when finished)	"0"

Bit number	Description	Default
Reg91, 0x5B		
D7	Unused	"0"
D6–D3	Channel "D" RF gain: FM / VHF / UHF / L / S "0000" –15.8 dB / –11.8 dB / –16.5 dB / –12.0 dB / –11.3 dB "0001" –13.4 dB / –9.4 dB / –14.2 dB / –9.9 dB / –9.4 dB "0010" –10.1 dB / –6.1 dB / –11.8 dB / –7.8 dB / –7.4 dB "0011" –7.7 dB / –3.8 dB / –9.2 dB / –5.7 dB / –5.4 dB "0100" –5.2 dB / –1.4 dB / –6.7 dB / –3.7 dB / –3.7 dB "0101" –2.0 dB / 1.8 dB / –4.5 dB / –2.3 dB / –3.2 dB "0110" 1.4 dB / 5.2 dB / –1.5 dB / 0 dB / –1.9 dB "0111" 4.0 dB / 7.8 dB / 1.7 dB / 2.8 dB / 0.3 dB "1000" 7.1 dB / 10.9 dB / 4.8 dB / 5.4 dB / 2.9 dB "1001" 9.9 dB / 14.9 dB / 10.3 dB / 8.9 dB / 10.0 dB "1010" 12.1 dB / 17.8 dB / 12.7 dB / 11.0 dB / 10.3 dB "1011" 14.9 dB / 20.7 dB / 15.2 dB / 13.4 dB / 12.0 dB "1100" 17.5 dB / 23.3 dB / 17.6 dB / 15.9 dB / 14.4 dB "1101" 20.7 dB / 26.7 dB / 19.9 dB / 18.9 dB / 15.9 dB "1110" 22.7 dB / 28.8 dB / 21.8 dB / 21.0 dB / 18.1 dB "1111" 22.7 dB / 28.8 dB / 21.8 dB / 21.0 dB / 18.1 dB ***Note:*** *Available if RF gain control is manual (if Reg91<D1–D0> is"00").*	"1110"
D2	Unused	"0"
D1–D0	Channel "D" RF gain control mode: "00" manual "01" automatic "10" external via pin #27 "11" not used	"00"
Reg92, 0x5C		
D7–D0	Channel "D" LPF cut-off frequency: "00000000" 2.6 MHz not guaranteed range … "00000101" 2.8 MHz not guaranteed range … "00001010" 3.1 MHz … "00010100" 3.6 MHz … "00101000" 4.5 MHz … "01000001" 5.6 MHz … "01011010" 6.6 MHz … "01110011" 7.5 MHz … "10010001" 8.5 MHz … "10110111" 9.3 MHz "10111001" 9.5 MHz not guaranteed range … "11111111" 10.8 MHz not guaranteed range	"10110111"

Bit number	Description	Default
Reg93, 0x5D		
D7	Unused	"0"
D6–D5	Channel "D" 2-bit ADC type: "0X" asynchronous "10" clocked by falling edge "11" clocked by rising edge	"10"
	Note: *Available if output data interface is 2-bit ADC (if Reg93<D2> is "1").*	
D4–D3	Channel "D" 2-bit ADC logic-level high: "00" 1.8V "01" 2.0V "10" 2.5V "11" VCC	"11"
	Note: *Available if output data interface is 2-bit ADC (if Reg93<D2> is "1").*	
D2	Channel "D" output data interface: "0" analog differential output "1" 2-bit ADC output	"1"
D1–D0	Channel "D" IFA gain control mode: "0X" manual "10" external via pins #38–39 "11" automatic	"11"
Reg94, 0x5E		
D7–D1	Unused	"0000000"
D0 (MSB)	Channel "D" IFA_I gain: "000000000" –6.34 dB … "000100000" –1.34 dB … "000111111" 4.14 dB … "001111111" 13.96 dB … "011011111" 28.89 dB … "100100000" 38.40 dB … "101100000" 48.27 dB … "110111111" 63.82 dB … "111111111" 73.74 dB	"0"
	Note: *Available if IF gain control is manual (if Reg93<D1–D0> is "0X").*	
Reg95, 0x5F		
D7–D0 (LSB)	Continue. Refer to Reg94<D0>.	"01111111"

Bit number	Description		Default
Reg96, 0x60			
D7–D1	Unused		"0000000"
D0 (MSB)	Channel "D" IFA_Q gain: "000000000" –6.34 dB … "000100000" –1.34 dB … "000111111" 4.14 dB … "001111111" 13.96 dB … "011011111" 28.89 dB … "100100000" 38.40 dB … "101100000" 48.27 dB … "110111111" 63.82 dB … "111111111" 73.74 dB ***Note:*** *Available if IF gain control is manual (if Reg93<D1–D0> is "0X").*		"0"
Reg97, 0x61			
D7–D0 (LSB)	Continue. Refer to Reg96<D0>.		"01111111"
Reg98, 0x62			
D7–D0	Channel "D" IFA_I output amplitude upper threshold control: "00000001" 5 mV … "00000010" 10 mV … "00100101" 50 mV … "01010000" 98 mV … "01010010" 100 mV … "10100000" 200 mV … "11000100" 299 mV … "11010100" 405 mV … "11011100" 512 mV … "11100010" 601 mV ***Note:*** *Available if output data interface is analog and IF gain control mode is automatic (if Reg93<D2> is "0" and Reg93<D1–D0> is "11").*	Channel "D" IFA_I digital detector upper threshold w.r.t sinewave signal: "00000000" 0% … "01010000" 31% … "01110011" 45% … "10011010" 60% … "11000000" 75% … "11111111" 99.6% ***Note:*** *Available if output data interface is 2-bit ADC and IF gain control mode is automatic (if Reg93<D2> is "1" and Reg93<D1–D0> is "11").*	"01010000"

<table>
<tr><th>Bit number</th><th colspan="2">Description</th><th>Default</th></tr>
<tr><td colspan="4">Reg99, 0x63</td></tr>
<tr><td rowspan="2">D7–D0</td><td>Channel “D” IFA_I output amplitude lower threshold control:
“00000001” 5 mV
…
“00000010” 10 mV
…
“00100101” 50 mV
…
“01000110” 87 mV
…
“01001100” 94 mV
…
“01010010” 100 mV
…
“10100000” 200 mV
…
“11000100” 299 mV
…
“11010100” 405 mV
…
“11011100” 512 mV
…
“11100010” 601 mV</td><td>Channel “D” IFA_I digital detector lower threshold w.r.t sinewave signal:
“00000000” 0%
…
“01000110” 27.3%
…
“01001100” 29.7%
…
“01110011” 45%
…
“10011010” 60%
…
“11000000” 75%
…
“11111111” 99.6%</td><td rowspan="2">“01000110”</td></tr>
<tr><td>Note: Available if output data interface is analog and IF gain control mode is automatic (if Reg93<D2> is “0” and Reg93<D1–D0> is “11”).</td><td>Note: Available if output data interface is 2-bit ADC and IF gain control mode is automatic (if Reg93<D2> is “1” and Reg93<D1–D0> is “11”).</td></tr>
<tr><td colspan="4">Reg100, 0x64</td></tr>
<tr><td rowspan="2">D7–D0</td><td>Channel “D” IFA_Q output amplitude upper threshold control:
“00000001” 5 mV
…
“00000010” 10 mV
…
“00100101” 50 mV
…
“01010000” 98 mV
…
“01010010” 100 mV
…
“10100000” 200 mV
…
“11000100” 299 mV
…
“11010100” 405 mV
…
“11011100” 512 mV
…
“11100010” 601 mV</td><td>Channel “D” IFA_Q digital detector upper threshold w.r.t sinewave signal:
“00000000” 0%
…
“01010000” 31%
…
“01110011” 45%
…
“10011010” 60%
…
“11000000” 75%
…
“11111111” 99.6%</td><td rowspan="2">“01010000”</td></tr>
<tr><td>Note: Available if output data interface is analog and IF gain control mode is automatic (if Reg93<D2> is “0” and Reg93<D1–D0> is “11”).</td><td>Note: Available if output data interface is 2-bit ADC and IF gain control mode is automatic (if Reg93<D2> is “1” and Reg93<D1–D0> is “11”).</td></tr>
</table>

<table>
<tr><th>Bit number</th><th colspan="2">Description</th><th>Default</th></tr>
<tr><td colspan="4">Reg101, 0x65</td></tr>
<tr><td rowspan="2">D7–D0</td><td>Channel “D” IFA_Q output amplitude lower threshold control:
“00000001” 5 mV
…
“00000010” 10 mV
…
“00100101” 50 mV
…
“01000110” 87 mV
…
“01001100” 94 mV
…
“01010010” 100 mV
…
“10100000” 200 mV
…
“11000100” 299 mV
…
“11010100” 405 mV
…
“11011100” 512 mV
…
“11100010” 601 mV</td><td>Channel “D” IFA_Q digital detector lower threshold w.r.t sinewave signal:
“00000000” 0%
…
“01000110” 27.3%
…
“01001100” 29.7%
…
“01110011” 45%
…
“10011010” 60%
…
“11000000” 75%
…
“11111111” 99.6%</td><td rowspan="2">“01000110”</td></tr>
<tr><td>Note: Available if output data interface is analog and IF gain control mode is automatic (if Reg93<D2> is “0” and Reg93<D1–D0> is “11”).</td><td>Note: Available if output data interface is 2-bit ADC and IF gain control mode is automatic (if Reg93<D2> is “1” and Reg93<D1–D0> is “11”).</td></tr>
<tr><td colspan="4">Reg102, 0x66</td></tr>
<tr><td>D7–D2</td><td colspan="2">Unused</td><td>“000000”</td></tr>
<tr><td rowspan="2">D1–D0</td><td colspan="2">Channel “D” IFA output DC level:
“00” 0.46×VCC
“01” 0.50×VCC
“10” 0.53×VCC
“11” 0.56×VCC</td><td rowspan="2">“01”</td></tr>
<tr><td colspan="2">Note: Available if output data interface is analog (if Reg93<D2> is “0”).</td></tr>
</table>

Calibration and test section:

– IQ phase correction

Bit number	Description	Default
Reg103, 0x67		
D7–D6	Unused	“00”
D5–D0	Channel “D” IQ phase correction for FM band: “000000” 76.3° … … “011111” 89.8° “100000” 90° “100001” 90.3° … … “111111” 106.2°	“011111”
Reg104, 0x68		
D7–D6	Unused	“00”
D5–D0	Channel “D” IQ phase correction for VHF band: “000000” 76° … … “011111” 89.8° “100000” 90° “100001” 90.2° … … “111111” 101.8°	“011111”
Reg105, 0x69		
D7–D6	Unused	“00”
D5–D0	Channel “D” IQ phase correction for UHF band: “000000” 74.3° … … “011111” 89.8° “100000” 90° “100001” 90.3° … … “111111” 105.7°	“011111”
Reg106, 0x6A		
D7	Unused	“0”
D6–D0	Channel “D” IQ phase correction for L and S bands: L band S band “0000000” 81.9° 77.4° “0000001” 82° 77.6° … … … “0111111” 89.9° 89.8° “1000000” 90° 90° “1000001” 90.1° 90.2° … … … “1111110” 97.8° 102.2° “1111111” 98° 102.4°	“0111111”

4. OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage _____ –0.5…+3.9 V
Maximum input signal level _____ +10 dBm
Operating temperature range _____ –40…+85°C
Storage temperature _____ –55…+125°C
Junction temperature _____ +150°C
Soldering temperature _____ +260°C
Thermal resistance:

- crystal-package _____ +28 °C/W

Electrostatic discharge rating:

- HBM (pins 9, 12, 14, 16, 74, 75, 91, 94, 96, 98, 101, 103, 105, 108)_____ 0.5 kV
- HBM (pins 20, 21, 22, 23, 25, 26, 29, 30, 32, 33, 52, 53)_____ 1kV
- HBM (except pins 9, 12, 14, 16, 20, 21, 22, 23, 25, 26, 29, 30, 32, 33, 52, 53, 74, 75, 91, 94, 96, 98, 101, 103, 105, 108)_____ 2 kV

4.1. DC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 V to 3.6V, T_a =–40…+85°C. Typical values are at V_{cc} = 3.0 V, T_a =+27°C, unless otherwise specified.

Parameter	Symbol	Condition		Value			Unit
				min	typ.	max	
Common							
Supply voltage	V_{cc}	–		2.8	3.0	3.6	V
Current consumption	I_{cc}	Mode 1.1 / Mode 1.2		–	98.3 / 103.1	–	mA
		Mode 2.1 / Mode 2.2		–	177.8 /182.3	–	
		Mode 3.1 / Mode 3.2		–	166.2 / 170.6	–	
		Mode 4.1 / Mode 4.2		–	36.7 / 38.7	–	
		Mode 5.1 / Mode 5.2		–	84.7 / 92.8	–	
		Mode 6.1 / Mode 6.2		–	71.9 / 80.0	–	
	I_{shd}	Shutdown		–	2	–	uA
Die temperature measurement range	T_j	–		–40	+25	+100	°C
Die temperature measurement resolution	ΔT_j	–		–	0.8	–	°C
Die temperature measurement accuracy	γT_j	–		–	±5	–	°C
Input logic-level low	V_{IL}	–		0	–	0.3	V
Input logic-level high	V_{IH}	–		V_{cc} – 0.3	–	V_{cc}	V
Output logic-level low	V_{OL}	I_{LOAD} = 100µA		0	–	0.3	V
Output logic-level high	V_{OH}	I_{LOAD} = 100µA		V_{cc} – 0.3	–	V_{cc}	V
Output logic-level high (ADC output)	V_{OH_ADC}	I_{LOAD} = 0 mA/2 mA	Preset 1	–	1.8 / 1.7	–	V
			Preset 2	–	2.0 / 1.9	–	
			Preset 3	–	2.5 / 2.4	–	
			Preset 4	–	V_{cc} / V_{cc} – 0.2	–	
Output logic-level low (ADC output)	V_{OL_ADC}	I_{LOAD} = 2 mA		0	0.04	0.2	V
ADCs external sampling frequency input DC level	V_{DC_FS}	ECL		0.5	–	V_{cc} – 0.5	V
Clock output DC level	V_{DC_CLK}	ECL	Preset 1	–	1.8 – V_{CLK}/4	–	V
			Preset 2	–	1.95 – V_{CLK}/4	–	
			Preset 3	–	2.7 – V_{CLK}/4	–	
			Preset 4	–	2.85 – V_{CLK}/4	–	
		LVDS		–	1.2	–	

Parameter	Symbol	Condition		Value			Unit
				min	typ.	max	
Channels "A", "B" and "C"							
Active antenna output voltage drop	ΔV_{AA}	From supply voltage V_{cc}. I_{AA}=10mA. Note 1		–	0.12	–	V
Short-circuit protection current	I_{AS}	Note 2	Tunable. Preset 4	–	16.0	–	mA
Active antenna detection current	I_{AW}	Note 3	Tunable. Preset 4	–	1.75	–	mA
IFA output DC level	$V_{DC\_IFA\_ABC}$	–		–	V_{cc} – 1.37	–	V
Channel "D"							
IFA output DC level	$V_{DC\_IFA\_D}$	Preset1		–	0.46×V_{cc}	–	V
		Preset2		–	0.50×V_{cc}	–	
		Preset3		–	0.53×V_{cc}	–	
		Preset4		–	0.56×V_{cc}	–	
RF gain control voltage	V_{RF_GC}	Maximum gain		–	V_{cc}	–	V
		Minimum gain		–	0	–	
IF gain control voltage	V_{IF_GC}	Maximum gain		–	(V_{cc} – 0.1)/2	–	V
		Minimum gain		–	0.05	–	

Notes:

1. Voltage drop value is evaluated from the equation $\Delta V = 0.1V + (2Ohm \times I_{AA})$, where I_{AA} is active antenna current.
2. Current $I_{AS} = I_{max}$, where I_{max} is active antenna maximal current (for Reg33<D7–D4> for Channel "A" / Reg55<D7–D4> for Channel "B"/ Reg77<D7–D4> for Channel "C" = "0011").
3. Current $I_{AW} = I_{min}$, where I_{min} is active antenna minimal current (for Reg33<D7–D4> for Channel "A" / Reg55<D7–D4> for Channel "B"/ Reg77<D7–D4> for Channel "C" = "0011").

Modes:

1. **3 channels and CLK output** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C)
2. **4 channels and CLK output** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C + S band or L2/L3/L5 band, IQ GNSS @ PLL D)
3. **4 channels and CLK output** (3 various combinations of L1/L2/L3/L5 bands, IQ GNSS @ PLL A, B, C + DGPS @ PLL D)
4. **1 channel (**L1/L2/L3/L5 band, IQ GNSS @ PLL A/B/C)
5. **1 channel (**S band or L2/L3/L5 band, IQ GNSS @ PLL D)
6. **1 channel (**DGPS @ PLL D)

*** .1** analog differential output
*** .2** 2-bit ADC output

4.2. AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 V to 3.6V, T_a =–40…+85°C. Typical values are at V_{cc} = 3.0 V, T_a =+27°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ	Value max	Unit
Common							
Reference frequency (TCXO) range	F_{REF}	–		10	10	50	MHz
Reference signal input level	REF_{IN}	Sine or triangle wave		0.8	1	2	Vp-p
ADCs external input sampling frequency	FS	Can be applied to pins #52–53		10	–	120	MHz
ADCs external sampling signal input level	FS_{IN}	ECL		0.4	–	–	Vp-p
		CMOS		0.4	–	1.2	
		LVDS		0.1	–	0.5	
Clock frequency	F_{CLK}	$F_{VCO}/2C = F_{LO}/C$, where C = Reg11<7:0>	LVDS	10	72.27	120	MHz
			CMOS			100	
Peak-to-peak voltage at the differential clock output	V_{CLK}	LVDS, R_{LOAD} = 100Ohm	Preset1	–	290	–	mVp-p
			Preset2	–	450	–	
			Preset3	–	600	–	
			Preset4	–	760	–	
		ECL, C_{LOAD} < 5pF	Preset1	–	420	–	mVp-p
			Preset2	–	550	–	
			Preset3	–	690	–	
			Preset4	–	770	–	
Output logic-level high at CMOS clock output	V_{OH_CLK}	CMOS, C_{LOAD} < 5pF	Preset1	–	1.8	–	V
			Preset2	–	1.95	–	
			Preset3	–	2.7	–	
			Preset4	–	2.85	–	
			Preset5	–	V_{CC} – 0.1	–	
Output logic-level low at CMOS clock output	V_{OL_CLK}	–		0	–	0.2	V

4.2.1. CHANNELS “A”, “B”, “C” AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 V to 3.6V, T_a =–40…+85°C. Typical values are at V_{cc} = 3.0 V, T_a =+27°C, unless otherwise specified.

Parameter	Symbol	Condition			Value min	Value typ	Value max	Unit
Overall								
Input frequency range	F_{IN_ABC}	L1 band			1530	–	1620	MHz
		L2, L3, L5 band			1150	–	1300	
Total maximum gain	G_{ABC}	Referred to LNA1 input	L1 band		–	102	–	dB
			L2, L3, L5 band		–	100	–	
		Referred to LNA2 input	L1 band		–	86	–	
			L2, L3, L5 band		–	84	–	
		Referred to mixer input			–	84	–	
Double sideband noise figure in IQ mode	NF_{ABC}	G_{IF} > 45dB	Referred to LNA1 input	L1 band	–	2.1	–	dB
				L2 band	–	2.1	–	
				L3, L5 band	–	1.9	–	
			Referred to LNA2 input		–	8.3		
			Referred to mixer input		–	4.3	–	
1dB compression point	P_{1dB_ABC}	G_{IF} = min	Referred to LNA1 input		–	–55	–	dBm
			Referred to LNA2 input		–	–38	–	
			Referred to mixer input		–	–37	–	

Parameter	Symbol	Condition		Value min	Value typ	Value max	Unit
LNA1							
LNA1 noise figure	NF_{LNA1}	–		–	1.1	–	dB
LNA1 gain	G_{LNA1}	L1 band		–	18	–	dB
		L2, L3, L5 band		–	16	–	
LNA1 input VSWR	$VSWR_{LNA1\_IN}$	L1 band	With matching circuit. @50Ohm	–	1.5	1.9	–
		L2, L3, L5 band		–	1.4	2.0	
LNA1 output VSWR	$VSWR_{LNA1\_OUT}$	L1 band	@50Ohm	–	1.4	1.9	–
		L2, L3, L5 band		–	1.7	2.3	
LNA1 input 1dB compression point	P_{1dB_LNA1}	L1 band		–	–20.5	–	dBm
		L2, L3, L5 band		–	–22.3	–	
LNA1 3rd order intercept point	$IIP3_{LNA1}$	L1 band		–	–10	–	dBm
		L2, L3, L5 band		–	–7	–	
LNA2							
LNA2 noise figure	NF_{LNA2}	–		–	4.6	–	dB
LNA2 gain	G_{LNA2}	L1 band		–	2	–	dB
		L2, L3, L5 band		–	0	–	
LNA2 input VSWR	$VSWR_{LNA2\_IN}$	L1 band	@50Ohm	–	1.3	1.4	–
		L2, L3, L5 band		–	1.6	1.7	
LNA2 output VSWR	$VSWR_{LNA2\_OUT}$	L1 band	@50Ohm	–	1.5	1.9	–
		L2, L3, L5 band		–	1.7	2.1	
LNA2 input 1dB compression point	$P_{1dB\ LNA2}$	L1 band		–	4	–	dBm
		L2, L3, L5 band		–	6	–	
LNA2 3rd order intercept point	$IIP3_{LNA2}$	L1 band		–	16	–	dBm
		L2, L3, L5 band		–	18	–	
Mixer&Polyphase filter							
Mixer&Polyphase filter gain	G_{MIX_ABC}	–		–	25	–	dB
Mixer input VSWR	$VSWR_{IN\_MIX\_ABC}$	L1 band	@50Ohm	–	2.0	–	–
		L2, L3, L5 band		–	4.3	–	
Image rejection	IR_{ABC}	Optionally. If Channel# mode ≠"00".		–	30	–	dB
LPF&IFA							
Output frequency range	F_{IF_ABC}	Tunable, assured/not guaranteed		2	–	30 / 37	MHz
LPF 3dB cut-off frequency	$F_{cut\_LPF\_ABC}$	Tunable, assured/not guaranteed		9 / 13	–	30 / 37	MHz
IF (LPF&IFA) minimum gain	$G_{IF\_MIN\_ABC}$	–		–	1.7	–	dB
IF (LPF&IFA) maximum gain	$G_{IF\_MAX\_ABC}$	–		–	59.2	–	dB
IF AGC range	ΔG_{IF_ABC}	Assured		–	57.5	–	dB
Stopband attenuation	S_{A_ABC}	$F_{cut\_LPF\_ABC}$ = 30MHz	F = 60 MHz	–	18	–	dB
			F = 90 MHz	–	30	–	
Sinusoidal/noise signal peak-to-peak voltage at the differential linear outputs	$V_{p\text{-}p\_ABC}$	510 Ohm load resistance. Note 1		–	230/ 570	–	mV
Output impedance	R_{out_ABC}	Analog differential output		–	510	–	Ohm
IQ phase imbalance	$\Delta\varphi_{ABC}$	–		–	±1	±3	degree
IQ amplitude output voltage imbalance	ΔA_{ABC}	–		–	–	20	mV
Group time delay ripple	ΔT_{GD_ABC}	F_{IF} = 2–9 MHz, F_{cut_LPF} = 9 MHz		–	10	–	ns
		F_{IF} = 2–30 MHZ, F_{cut_LPF} = 30 MHz		–	11	–	
ADC							
ADC resolution	R_{ADC}	–		–	2	–	bit
Output logic-level high (ADC output)	V_{OH_ADC}	I_{LOAD}=0mA/2mA	Preset 1	–	1.8 / 1.7	–	V
			Preset 2	–	2.0 / 1.9	–	
			Preset 3	–	2.5 / 2.4	–	
			Preset 4	–	V_{cc} / V_{cc}–0.2	–	

Parameter	Symbol	Condition			Value min	Value typ	Value max	Unit
Synthesizer								
LO frequency range	F_{LO_ABC}	L1 band			1550	–	1615	MHz
		L2, L3, L5 band			1160	–	1300	
VCO frequency range	F_{VCO_ABC}	L1 band			3100	–	3230	MHz
		L2, L3, L5 band			2320	–	2600	
PFD frequency range	F_{CMP_ABC}	–			5	–	50	MHz
VCO to PFD frequency integer-valued division ratio	N_{ABC}	–			16	–	4095	–
VCO to PFD frequency fractional-valued division resolution	F_{ABC}	–			–	24	–	Bit
Quadrature former division ratio	QF_{ABC}	–			–	2	–	–
VCO to CLK frequency integer-valued division ratio	C_{ABC}	–			4	–	255	–
TCXO to PFD frequency integer-valued division ratio	R_{ABC}	–			1	–	31	–
LO phase noise	PN_{LO_ABC}	Integer-N/Fractional-N, F_{LO}=1590MHz/1589MHz, F_{PFD}=10MHz		At 10 kHz offset	–	–97/–96	–	dBc/Hz
				At 100 kHz offset	–	–93/–93	–	
				At 1 MHz offset	–	–117/–105	–	
		Integer-N/Fractional-N, F_{LO}=1575MHz/1589MHz, F_{PFD}=50MHz		At 10 kHz offset	–	–102/–102	–	
				At 100 kHz offset	–	–103/–103	–	
				At 1 MHz offset	–	–114/–115	–	
		Integer-N/Fractional-N, F_{LO}=1235MHz/1234MHz, F_{PFD}=10MHz		At 10 kHz offset	–	–99/–99	–	
				At 100 kHz offset	–	–96/–96	–	
				At 1 MHz offset	–	–119/–104	–	
		Integer-N/Fractional-N, F_{LO}=1225MHz/1234MHz, F_{PFD}=50MHz		At 10 kHz offset	–	–106/–105	–	
				At 100 kHz offset	–	–107/–107	–	
				At 1 MHz offset	–	–117/–117	–	
		Integer-N/Fractional-N, F_{LO}=1190MHz/1189MHz, F_{PFD}=10MHz		At 10 kHz offset	–	–100/–100	–	
				At 100 kHz offset	–	–97/–97	–	
				At 1 MHz offset	–	–121/–106	–	
		Integer-N/Fractional-N, F_{LO}=1175MHz/1189MHz, F_{PFD}=50MHz		At 10 kHz offset	–	–106/–106	–	
				At 100 kHz offset	–	–107/–107	–	
				At 1 MHz offset	–	–118/–119	–	
LO RMS jitter	J_{RMS_ABC}	Integrated BW=100MHz. Integer-N/ Fractional-N.	F_{PFD}= 10MHz	L1 band	–	1.5/2.0	–	ps
				L2, L3, L5 bands	–	1.4/2.0	–	
			F_{PFD}= 50MHz	L1 band	–	0.9/0.9	–	
				L2, L3, L5 bands	–	0.9/0.9	–	

Note 1: RMS value measured. $V_{p\text{-}p\ sin} = V_{RMS} \times 2\sqrt{2}$; $V_{p\text{-}p\ noise} = V_{RMS} \times 6.6$. In Channel "D" Vp-p noise can be calculated only for signals in L2/S band.

4.2.2. CHANNEL "D" AC ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 V to 3.6V, T_a =–40…+85°C. Typical values are at V_{cc} = 3.0 V, T_a =+27°C, unless otherwise specified.

Parameter	Symbol	Condition		Value min	Value typ	Value max	Unit
Overall							
Input frequency range	F_{IN_D}	FM	Input pins #22-23	65	–	110	MHz
		VHF		160	–	240	
		UHF		470	–	862	
		L2, L3, L5 band	Input pins #20-21	1160	–	1300	
		S band		2470	–	2510	
Total maximum gain	G_D	FM		–	92.7	–	dB
		VHF		–	98.8	–	
		UHF		–	91.8	–	
		L2, L3, L5 band		–	91	–	
		S band		–	88.1	–	
Double sideband noise figure	NF_D	FM	G_{RF} = max, G_{IF} > 45dB	–	3.5	–	dB
		VHF		–	3.5	–	
		UHF		–	5.0	–	
		L2, L3, L5 band		–	4.2	–	
		S band		–	5.8	–	
1dB compression point	P_{1dB_D}	FM	G_{RF} = max, G_{IF} = min	–	–34	–	dBm
		VHF		–	–33	–	
		UHF		–	–39	–	
		L2, L3, L5 band		–	–29	–	
		S band		–	–26.5	–	
Input VSWR	$VSWR_{IN\_D}$	FM	@50Ohm	–	1.1	1.3	–
		VHF		–	1.2	1.4	
		UHF		–	1.8	2.8	
		L2, L3, L5 band		–	2.0	2.1	
		S band		–	1.3	1.5	
LNA&Mixer							
RF AGC range	ΔG_{RF_D}	FM		–	38.4	–	dB
		VHF		–	40.6	–	
		UHF		–	38.2	–	
		L2, L3, L5 band		–	32.9	–	
		S band		–	29.4	–	
LPF&IFA							
Output frequency range	F_{IF_D}	Tunable, assured/ not guaranteed	C23, C24 = 100nF	0.05	–	9.5 / 11	MHz
			C23, C24 = 4.7µF	0.0005	–		
LPF 3dB cut-off frequency	$F_{cut\_LPF\_D}$	Tunable, assured/not guaranteed		2.6 / 3	–	9.5 / 11	MHz
IFA minimum gain	$G_{IFA\_MIN\_D}$	–		–	–6	–	dB
IFA maximum gain	$G_{IFA\_MAX\_D}$	–		–	70	74	dB
IFA AGC range	ΔG_{IFA_D}	Assured		–	76	–	dB
Stopband attenuation	S_{A_D}	$F_{cut\_LPF\_D}$ =11 MHz	F = 22 MHz	–	40	–	dB
			F = 33 MHz	–	70	–	
Sinusoidal signal peak-to-peak voltage at the differential linear outputs	$V_{p\text{-}p\_D}$	Minimal	Note 1	–	50	–	mV
		Default		–	350	–	
		Maximal		–	1200	–	
Output impedance	R_{out_D}	Analog differential output		–	1.5	–	kOhm
IQ amplitude output voltage imbalance	ΔA_D	$V_{p\text{-}p\_D}$ = 50 mV		–	12	–	mV
		$V_{p\text{-}p\_D}$ = 430 mV		–	35	–	
		$V_{p\text{-}p\_D}$ = 1200 mV		–	45	–	
Group time delay ripple	ΔT_{GD_D}	F_{IF} = 0.05–3 MHz, $F_{cut\_LPF\_D}$ = 3 MHz		–	150	–	ns
		F_{IF} = 0.05–11MHz, $F_{cut\_LPF\_D}$ = 11 MHz		–	50	–	

Parameter	Symbol	Condition		Value min	Value typ	Value max	Unit
IQ phase imbalance	$\Delta\varphi_D$	–		–	±2	–	degree
ADC							
ADC resolution	R_{ADC}	–		–	2	–	bit
Output logic-level high (ADC output)	V_{OH_ADC}	I_{LOAD}=0 mA/2 mA	Preset 1	–	1.8 / 1.7	–	V
			Preset 2	–	2.0 / 1.9	–	
			Preset 3	–	2.5 / 2.4	–	
			Preset 4	–	V_{cc} /V_{cc}–0.2	–	
Synthesizer							
LO frequency range	F_{LO_D}	FM		65	–	110	MHz
		VHF		160	–	240	
		UHF		470	–	862	
		L2, L3, L5 band		1170	–	1290	
		S band		2480	–	2500	
VCO frequency range	F_{VCO_D}	VCO 1	FM, VHF, UHF	900	–	1300	MHz
		VCO 2		1250	–	1820	
		VCO 3	L2, L3, L5 band and S band	4680	–	5160	
PFD frequency range	F_{CMP_D}	–		5	–	50	MHz
VCO to PFD frequency integer-valued division ratio	N_D	FM, VHF, UHF		16	–	1023	–
		L2, L3, L5 band and S band		56	–	2047	
VCO to PFD frequency fractional-valued division resolution	F_D	–		–	24	–	bit
Quadrature former division ratio	QF_D	–		–	2	–	–
VCO to LO frequency integer-valued preliminary division ratio	QF_{PREDIV_D}	FM		–	8	–	–
		VHF	160–227.5 MHz	–	4	–	
			225–240 MHz	–	2	–	
		UHF		–	1	–	
		L2, L3, L5 band		–	2	–	
		S band		–	1	–	
TCXO to PFD frequency integer-valued division ratio	R_D	–		1	–	31	–
LO phase noise	PN_{LO_D}	Integer-N/Fractional-N, F_{LO}=93.75MHz, F_{PFD}=10MHz	At 10 kHz offset	–	–119/–119	–	dBc/Hz
			At 100 kHz offset	–	–116/–115	–	
			At 1 MHz offset	–	–137/–123	–	
		Integer-N/Fractional-N, F_{LO}=93.75MHz, F_{PFD}=50MHz	At 10 kHz offset	–	–123/–124	–	
			At 100 kHz offset	–	–120/–121	–	
			At 1 MHz offset	–	–136/–136	–	
		Integer-N/Fractional-N, F_{LO}=187.5MHz, F_{PFD}=10MHz	At 10 kHz offset	–	–113/–113	–	
			At 100 kHz offset	–	–110/–109	–	
			At 1 MHz offset	–	–131/–117	–	
		Integer-N/Fractional-N, F_{LO}=187.5MHz, F_{PFD}=50MHz	At 10 kHz offset	–	–117/–118	–	
			At 100 kHz offset	–	–114/–115	–	
			At 1 MHz offset	–	–130/–130	–	
		Integer-N/Fractional-N, F_{LO}=500MHzMHz, F_{PFD}=10MHz	At 10 kHz offset	–	–105/–104	–	
			At 100 kHz offset	–	–101/–100	–	
			At 1 MHz offset	–	–122/–105	–	
		Integer-N/Fractional-N, F_{LO}=500MHz, F_{PFD}=50MHz	At 10 kHz offset	–	–110/–108	–	
			At 100 kHz offset	–	–107/–106	–	
			At 1 MHz offset	–	–122/–121	–	
		Integer-N/Fractional-N, F_{LO}=1245MHz/1246MHz, F_{PFD}=10MHz	At 10 kHz offset	–	–98/–98	–	
			At 100 kHz offset	–	–96/–95	–	
			At 1 MHz offset	–	–122/–112	–	
		Integer-N/Fractional-N, F_{LO}=1237.5MHz/1246MHz F_{PFD}=50MHz	At 10 kHz offset	–	–102/–101	–	
			At 100 kHz offset	–	–102/–101	–	
			At 1 MHz offset	–	–122/–122	–	
		Integer-N/Fractional-N, F_{LO}=2490MHz/2492MHz, F_{PFD}=10MHz	At 10 kHz offset	–	–92/–92	–	
			At 100 kHz offset	–	–90/–89	–	
			At 1 MHz offset	–	–116/–106	–	

Parameter	Symbol	Condition			Value			Unit
					min	typ	max	
LO phase noise	PN_{LO_D}	Integer-N/Fractional-N, F_{LO}=2475MHz/2492MHz, F_{PFD}=50MHz		At 10 kHz offset	–	–96/–95	–	dBc/Hz
				At 100 kHz offset	–	–96/–95	–	
				At 1 MHz offset	–	–116/–116	–	
LO RMS jitter	J_{RMS_D}	Integrated BW=100MHz. Integer-N/ Fractional-N.	F_{PFD}= 10MHz	FM, VHF, UHF	–	2.0/3.5	–	ps
				L, S bands	–	1.6/1.8	–	
			F_{PFD}= 50MHz	FM, VHF, UHF	–	1.4/1.6	–	
				L, S bands	–	1.2/1.2	–	

Note 1: RMS value measured. $V_{p\text{-}p\ sin} = V_{RMS} \times 2\sqrt{2}$; $V_{p\text{-}p\ noise} = V_{RMS} \times 6.6$. In Channel “D” Vp-p noise can be calculated only for signals in L2/S band.

5. TYPICAL CHARACTERISTICS

5.1. TYPICAL CHARACTERISTICS

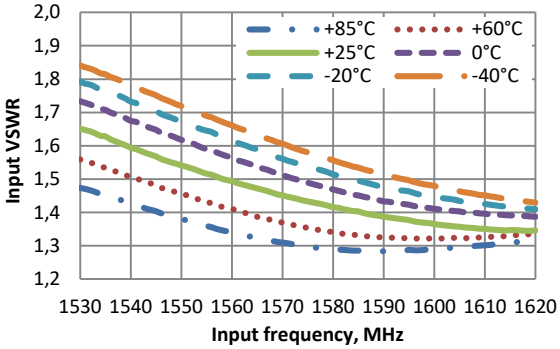


Figure 5.1: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; LNA1 input; L1 band

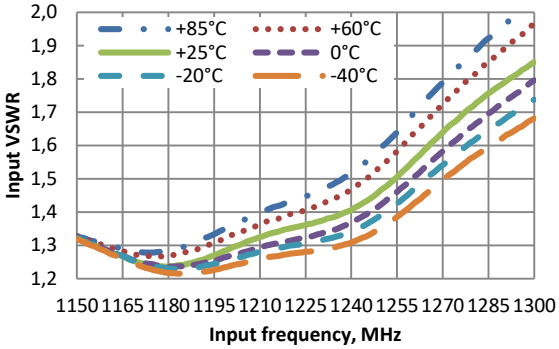


Figure 5.2: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; LNA1 input; L2, L3, L5 bands

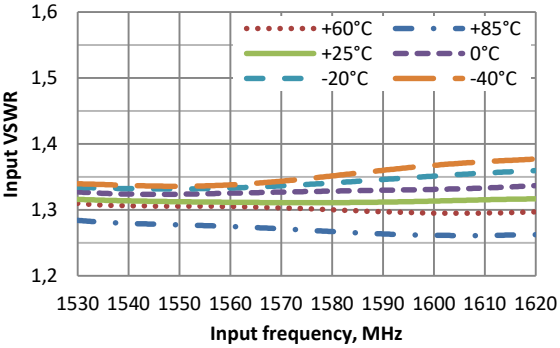


Figure 5.3: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; LNA2 input; L1 band

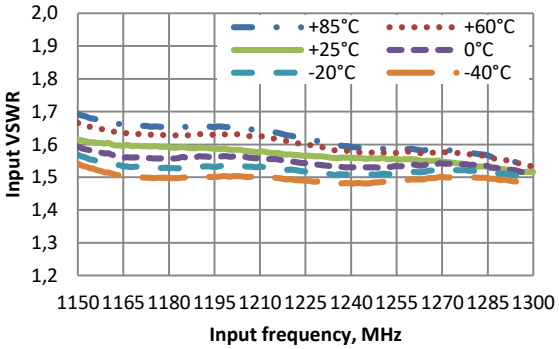


Figure 5.4: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; LNA2 input; L2, L3, L5 bands

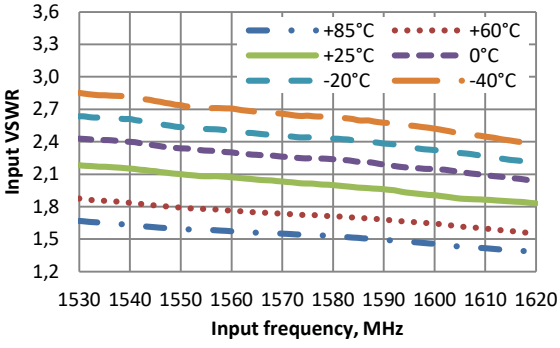


Figure 5.5: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; mixer input; L1 band

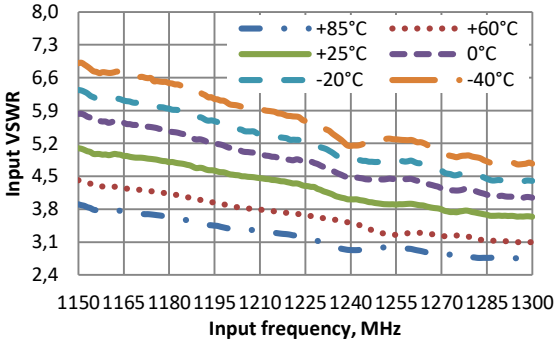


Figure 5.6: Input VSWR vs. Input frequency
Conditions: Channels “A”, “B”, “C”; mixer input; L2, L3, L5 bands

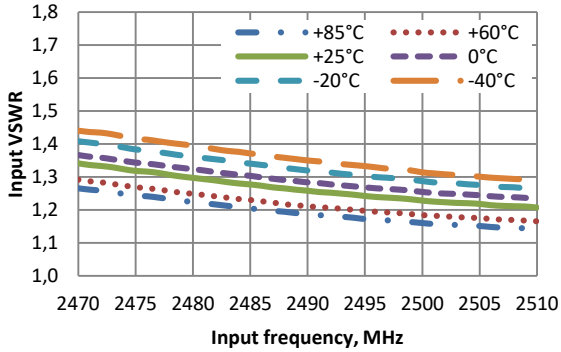


Figure 5.7: Input VSWR vs. Input frequency
Conditions: Channel “D”; S band

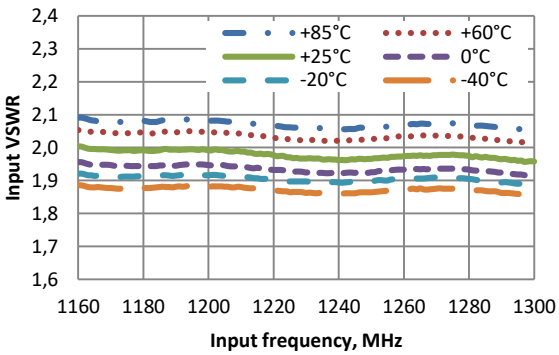


Figure 5.8: Input VSWR vs. Input frequency
Conditions: Channel “D”; L2, L3, L5 bands

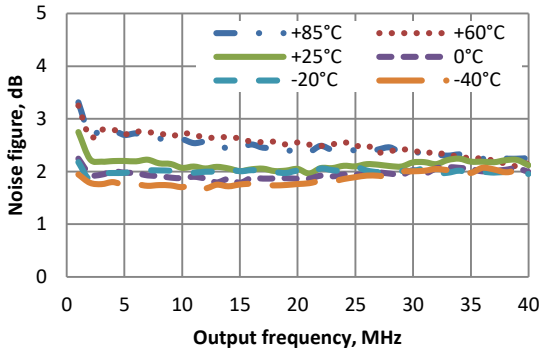


Figure 5.9:Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; LNA1 input; L1 band

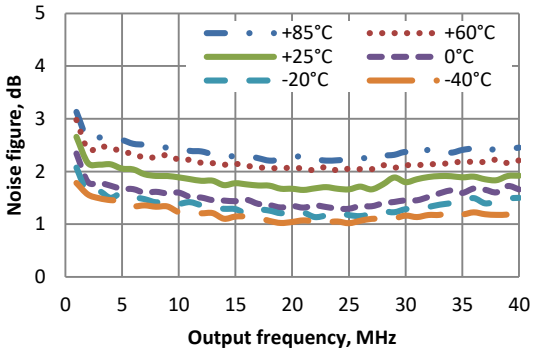


Figure 5.10:Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; LNA1 input; L2, L3, L5 band

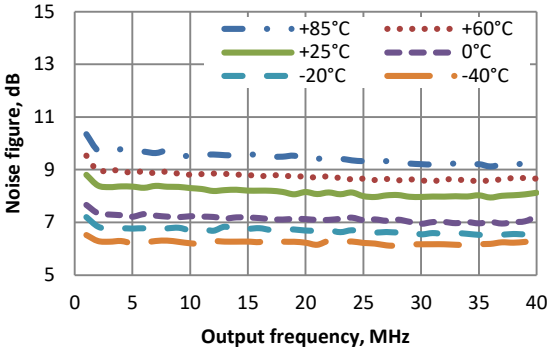


Figure 5.11:Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; LNA2 input; L1 band

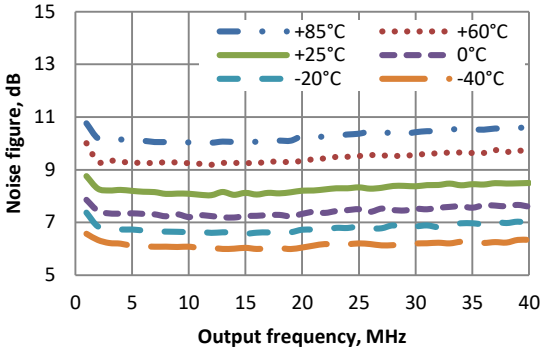


Figure 5.12:Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; LNA2 input; L2, L3, L5 bands

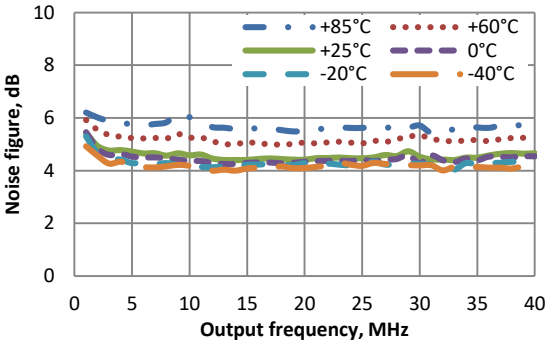


Figure 5.13: Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; mixer input; L1 band

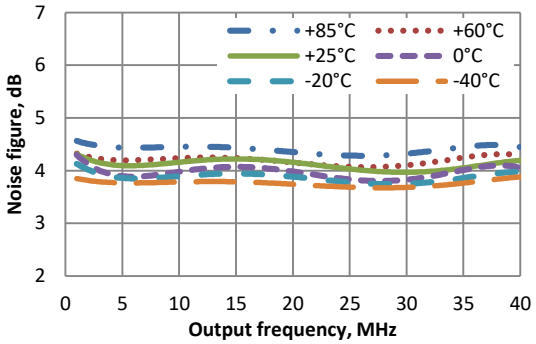


Figure 5.14: Double sideband noise figure vs. Output frequency
Conditions: Channels “A”, “B”, “C”; mixer input; L2, L3, L5 bands

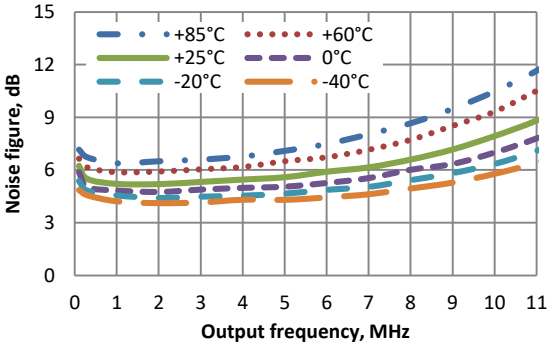


Figure 5.15: Double sideband noise figure vs. Output frequency
Conditions: Channel “D”; S band

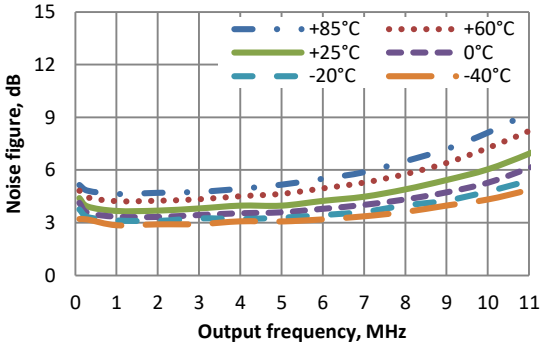


Figure 5.16: Double sideband noise figure vs. Output frequency
Conditions: Channel “D”; L2, L3, L5 bands

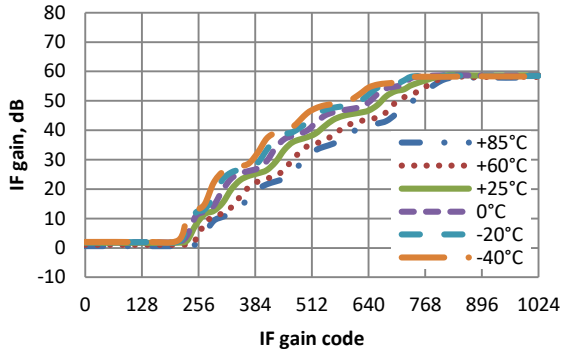


Figure 5.17: IF gain vs. IF gain code
Conditions: Channels “A”, “B”, “C”

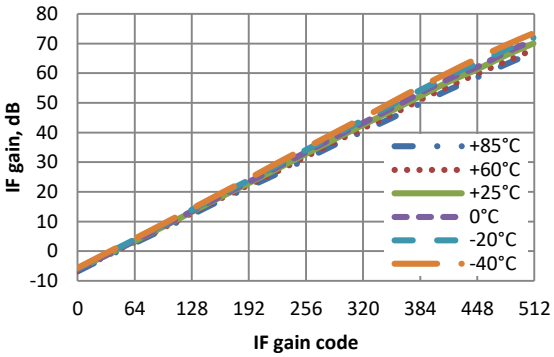


Figure 5.18: IF gain vs. IF gain code
Conditions: Channel “D”

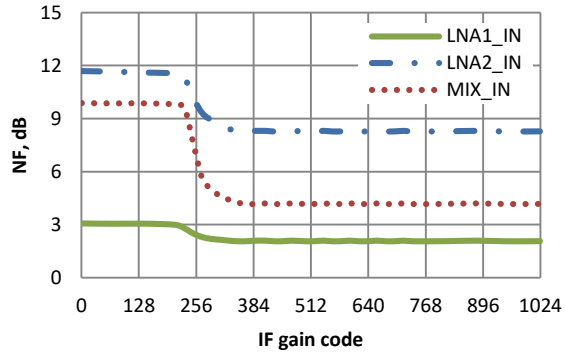


Figure 5.19: Double sideband noise figure vs. IF gain code
Conditions: Channels “A”, “B”, “C”

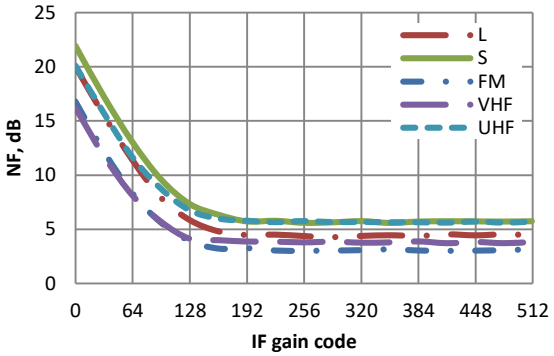


Figure 5.20: Double sideband noise figure vs. IF gain code
Conditions: Channel “D”, RF gain code ‘14’

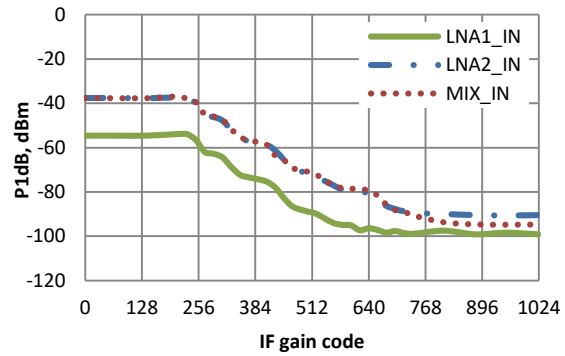


Figure 5.21: 1dB compression point vs. IF gain code
Conditions: Channels “A”, “B”, “C”

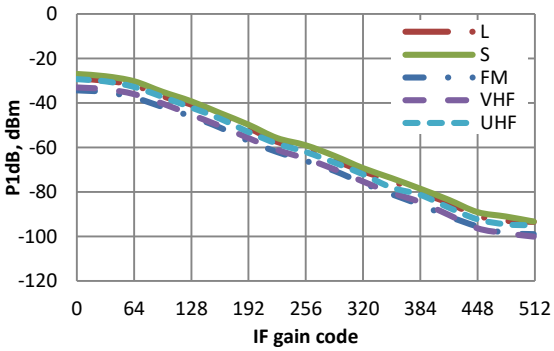


Figure 5.22: 1dB compression point vs. IF gain code
Conditions: Channel “D”, RF gain code ‘14’

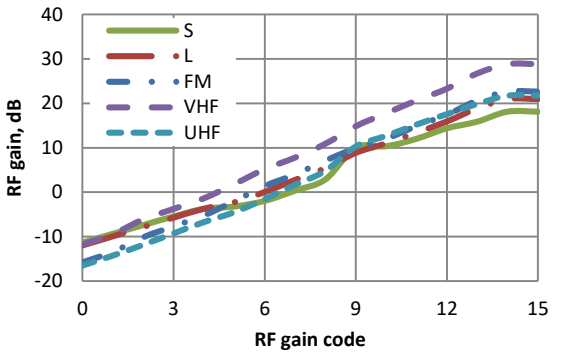


Figure 5.23: RF gain vs. RF gain code
Conditions: Channel “D”

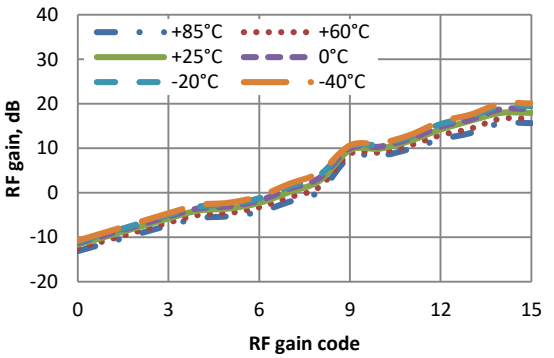


Figure 5.24: RF gain vs. RF gain code
Conditions: Channel “D”, S band

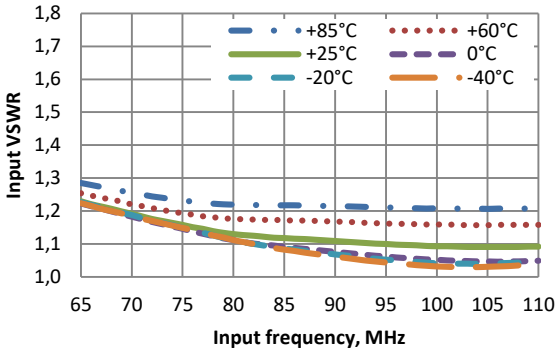


Figure 5.25: Input VSWR vs. Input frequency
Conditions: Channel "D"; FM band

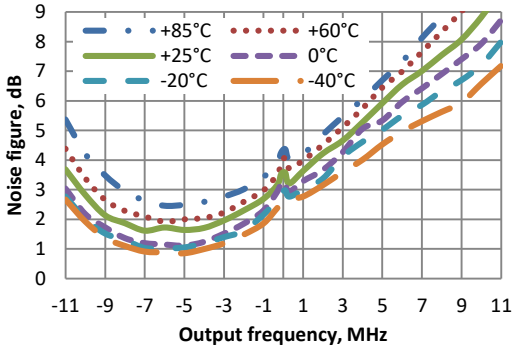


Figure 5.26: Double sideband noise figure vs. Output frequency
Conditions: Channel "D"; FM band

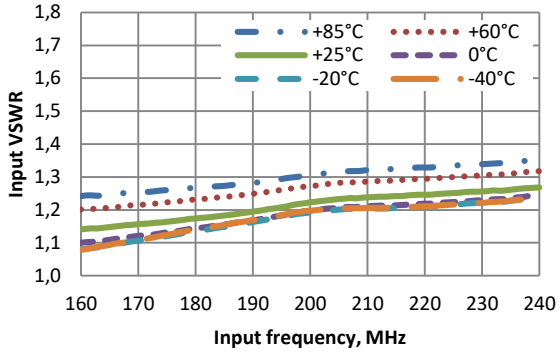


Figure 5.27: Input VSWR vs. Input frequency
Conditions: Channel "D"; VHF band

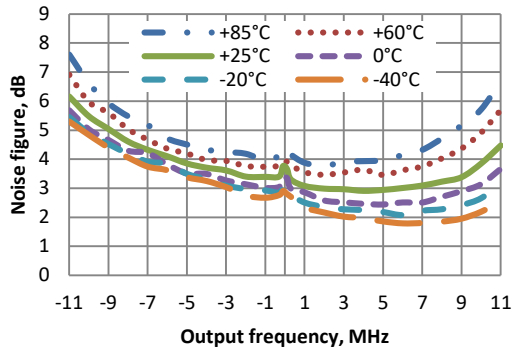


Figure 5.28: Double sideband noise figure vs. Output frequency
Conditions: Channel "D"; VHF band

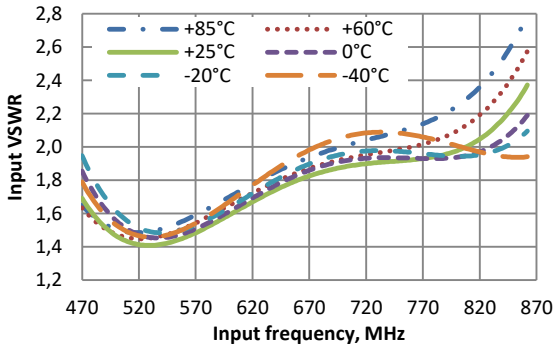


Figure 5.29: Input VSWR vs. Input frequency
Conditions: Channel "D"; UHF band

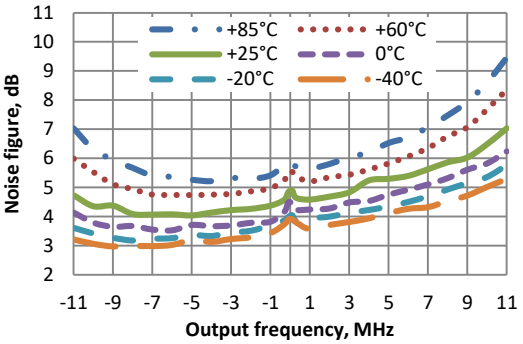


Figure 5.30: Double sideband noise figure vs. Output frequency
Conditions: Channel "D"; UHF band

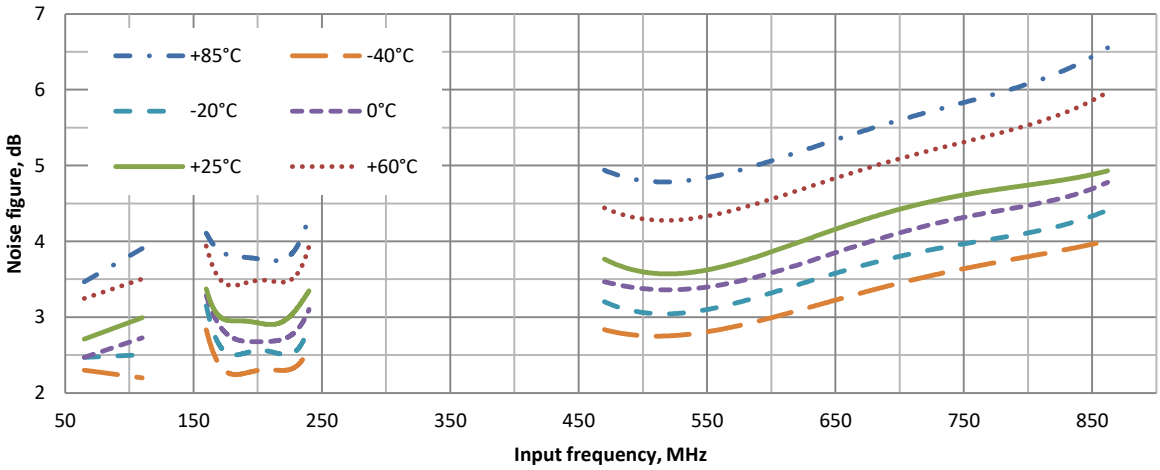


Figure 5.31: Double sideband noise figure vs. Input frequency
Conditions: Channel "D"; FM, VHF, UHF bands

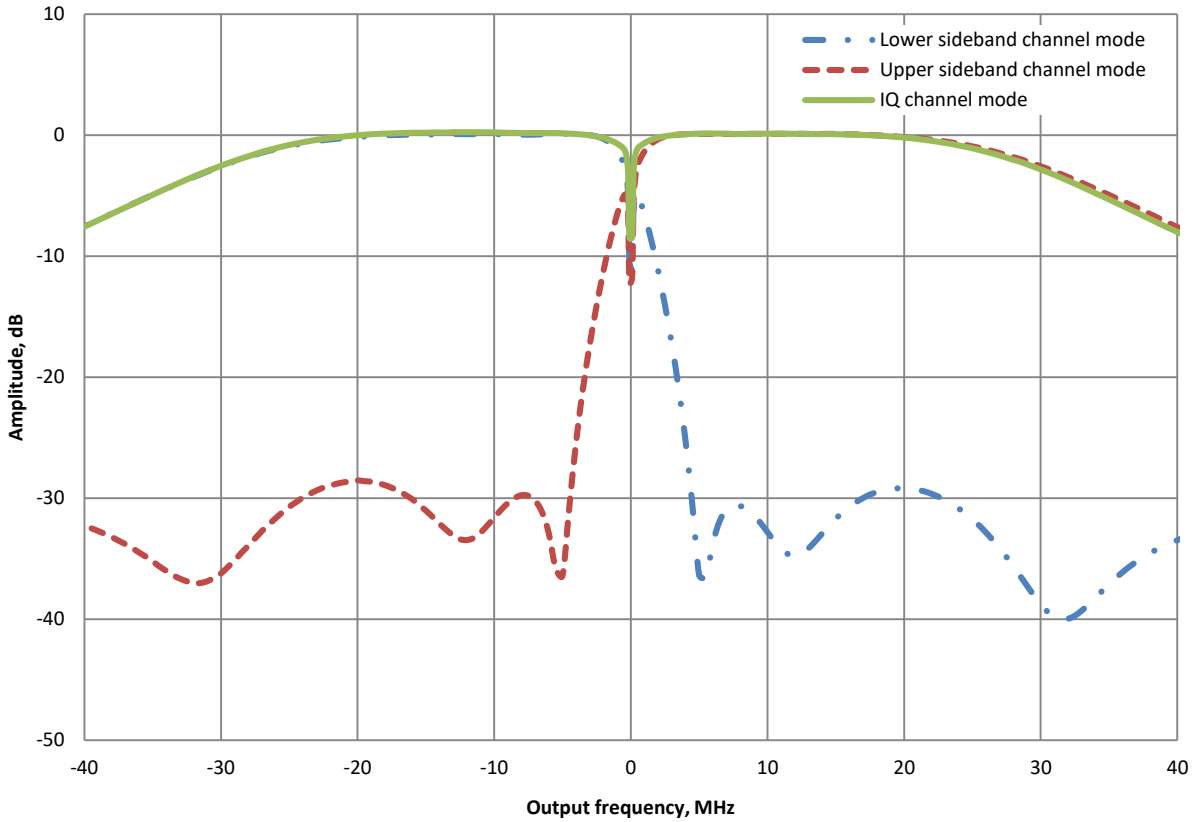


Figure 5.32: Frequency response (normalized)
Conditions: Channels “A”, “B”, “C”, LPF cut-off frequency 29.7MHz (code 89, default)

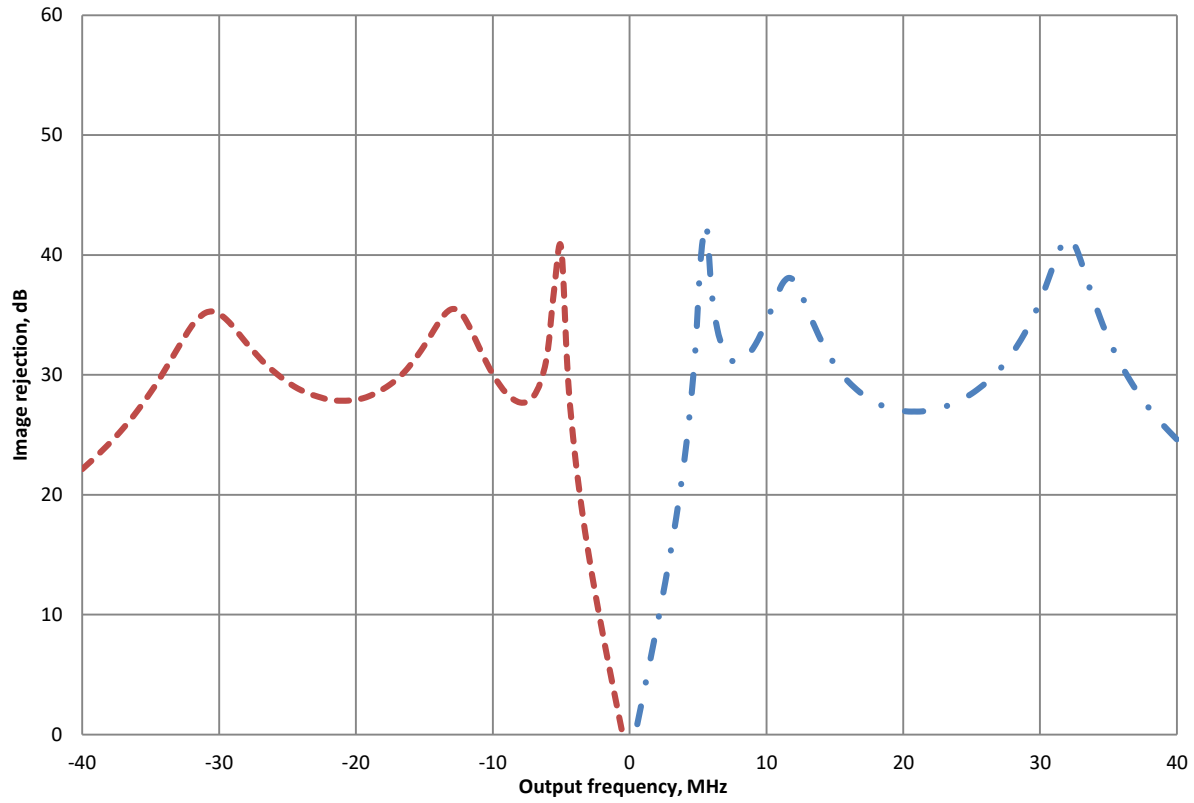


Figure 5.33: Image rejection
Conditions: Channels “A”, “B”, “C”

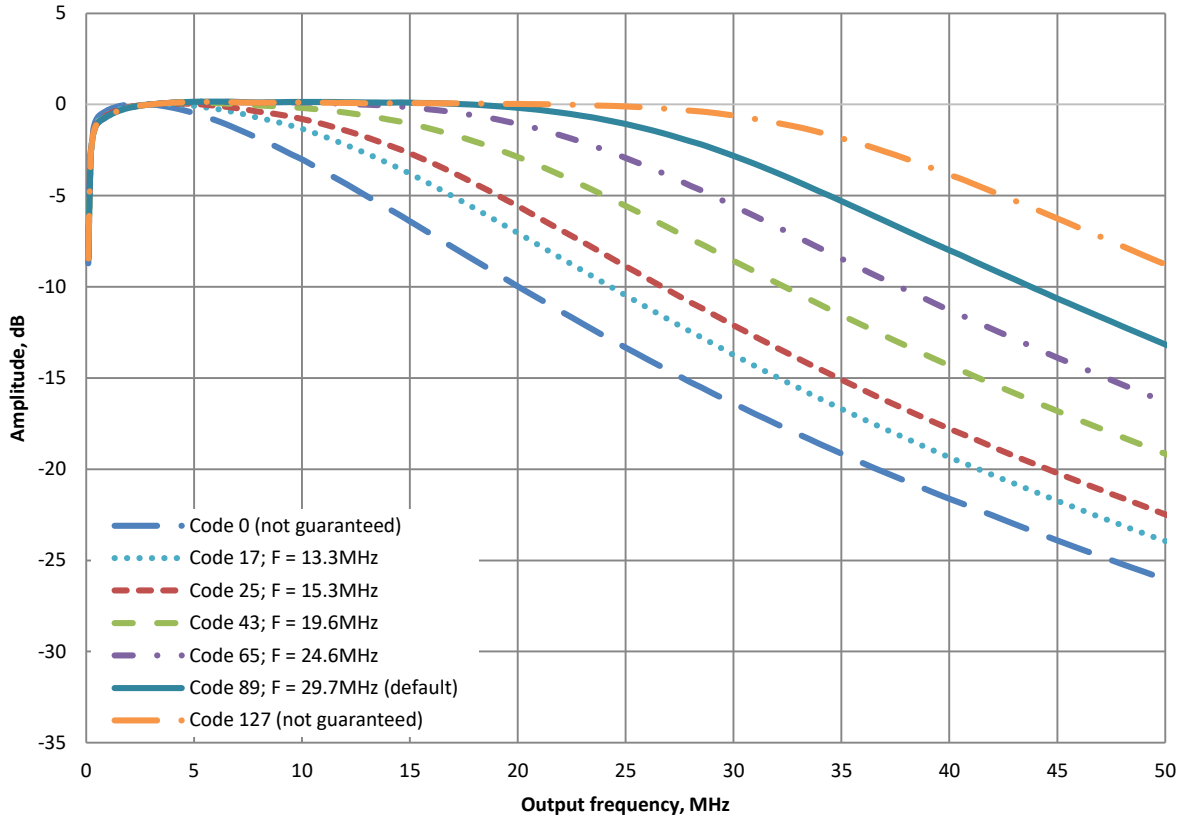


Figure 5.34: Frequency response (normalized)
Conditions: Channels “A”, “B”, “C”

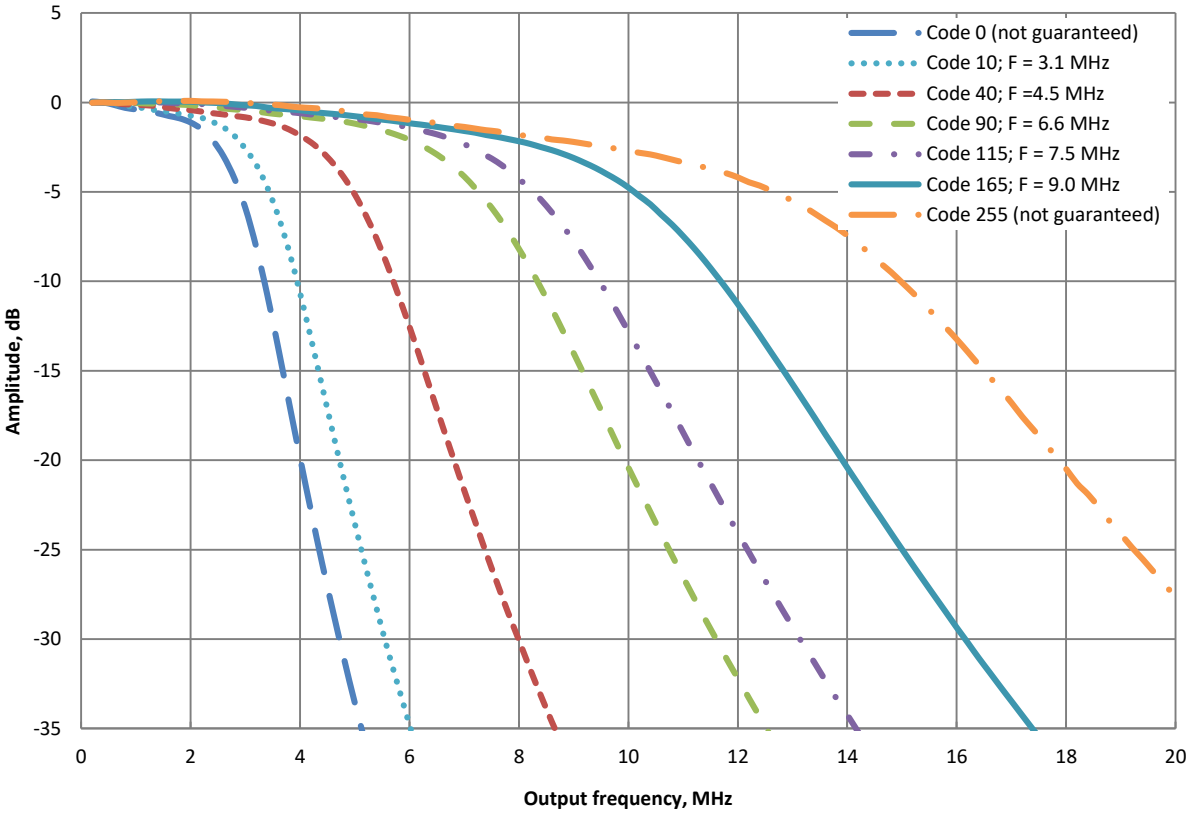


Figure 5.35: Frequency response (normalized)
Condition: Channels “D”

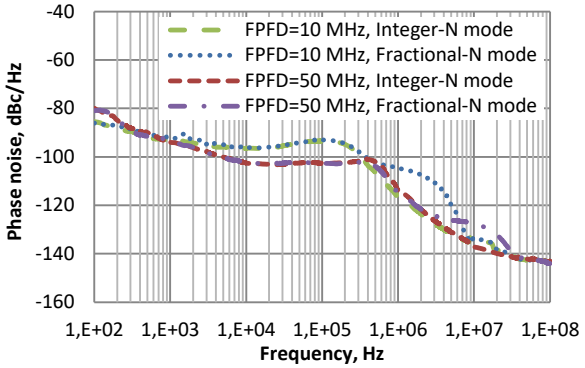


Figure 5.36: LO phase noise
Conditions: Channels "A", "B", C"; L1 band

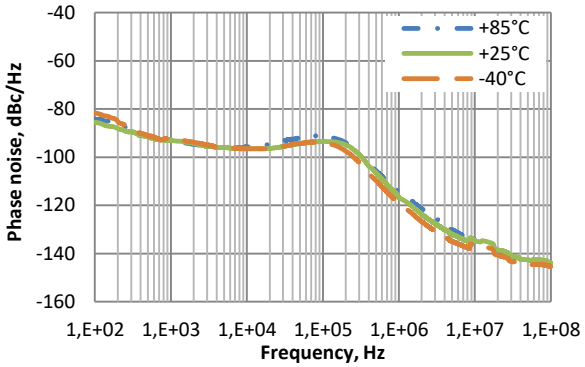


Figure 5.37: LO phase noise
Conditions: Channels "A", "B", C"; L1 band, F_{LO}=1590MHz;
Integer-N mode, F_{PFD}=10MHz

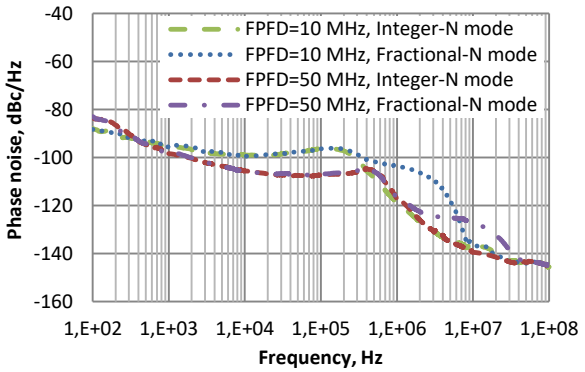


Figure 5.38: LO phase noise
Conditions: Channels "A", "B", C"; L2/L3/L5 band

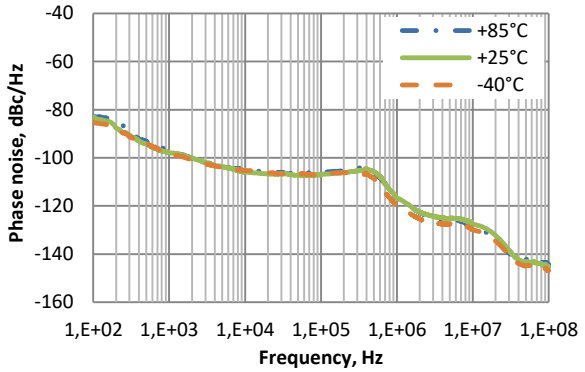


Figure 5.39: LO phase noise
Conditions: Channels "A", "B", C"; L2 band, F_{LO}=1235MHz;
Fractional-N mode, F_{PFD}=50MHz

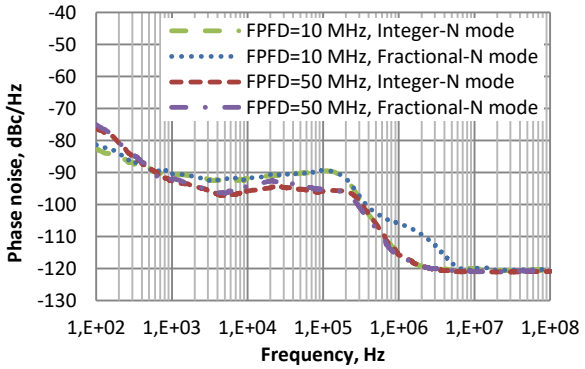


Figure 5.40: LO phase noise
Conditions: Channel "D"; S band

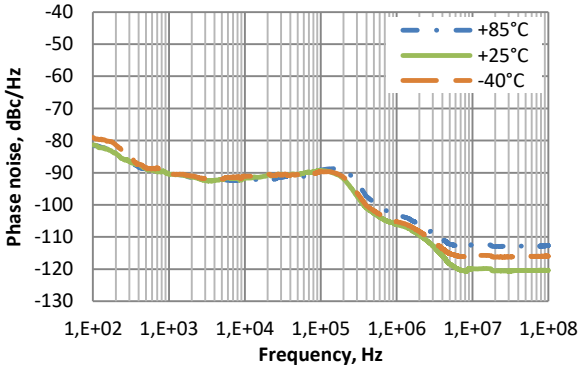


Figure 5.41: LO phase noise
Conditions: Channel "D"; S band, F_{LO}=2492MHz;
Fractional-N mode, F_{PFD}=10MHz

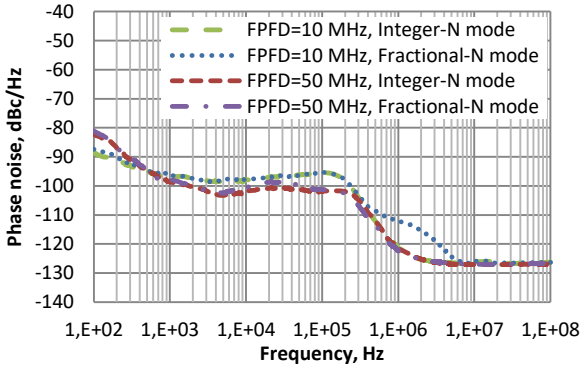


Figure 5.42: LO phase noise
Conditions: Channel "D"; L2/L3/L5 band

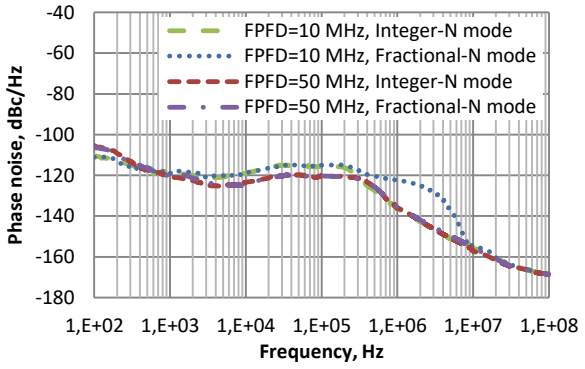


Figure 5.43: LO phase noise
Conditions: Channel "D"; FM band

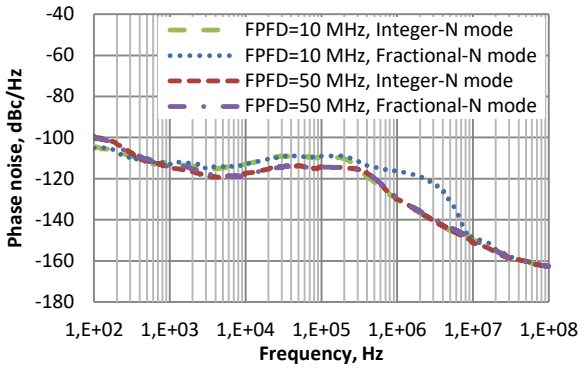


Figure 5.44: LO phase noise
Conditions: Channel "D"; VHF band

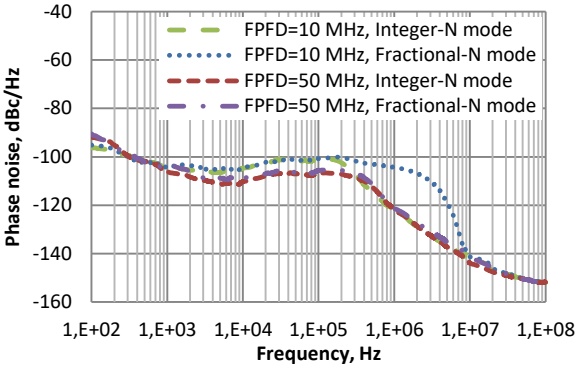


Figure 5.45: LO phase noise
Conditions: Channel "D"; UHF band

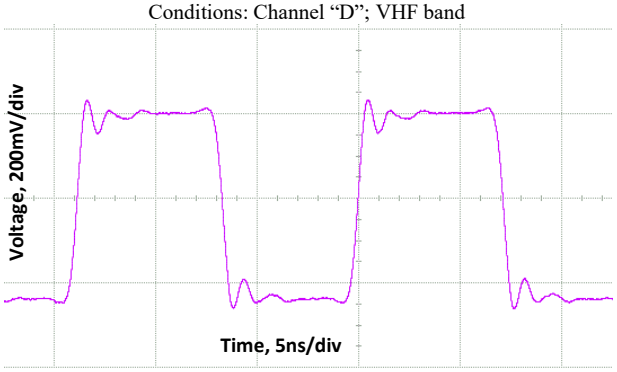


Figure 5.46: Typical clock output
Conditions: LVDS output type, R_{LOAD}=100Ohm,
V_{CLK} = 450mVp-p, F_{CLK} = 72.27MHz

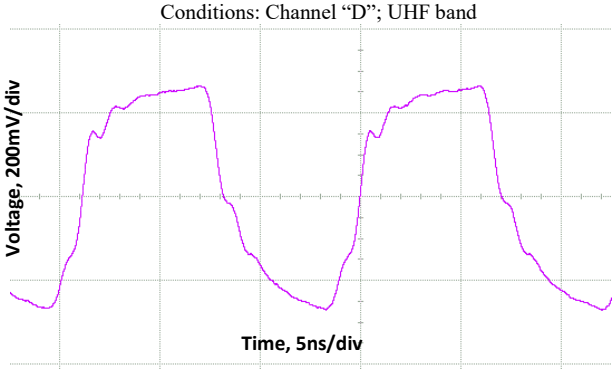


Figure 5.47: Typical clock output
Conditions: ECL output type, V_{CLK} = 550mVp-p, F_{CLK} = 72.27MHz

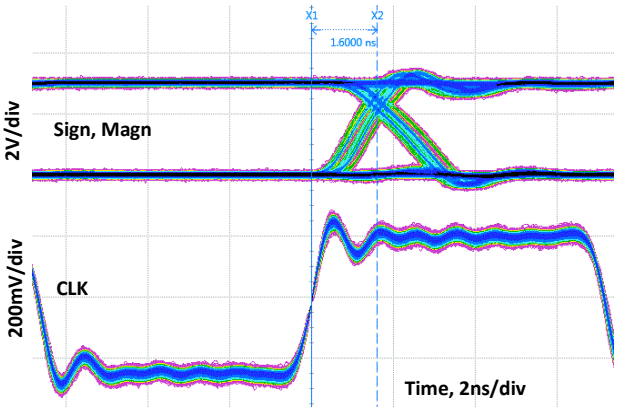


Figure 5.48: ADC output time diagram
Conditions: ADC clocked by rising edge, V_{OH_ADC} = VCC;
LVDS CLK output type, V_{CLK} = 450mVp-p

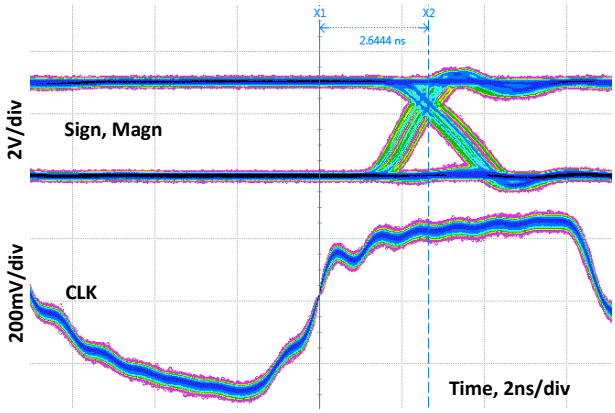


Figure 5.49: ADC output time diagram
Conditions: ADC clocked by rising edge, V_{OH_ADC} = VCC;
ECL CLK output type, V_{CLK} = 550mVp-p

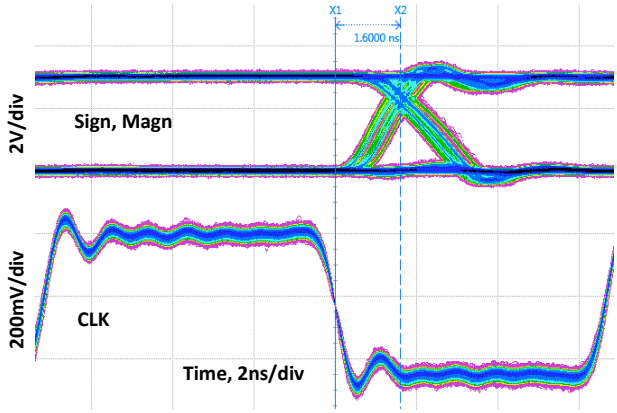


Figure 5.50: ADC output time diagram
Conditions: ADC clocked by falling edge, V_{OH_ADC} = VCC;
LVDS CLK output type, V_{CLK} = 450mVp-p

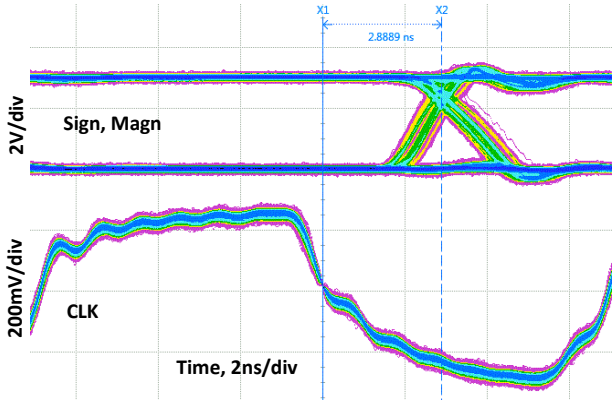


Figure 5.51: ADC output time diagram
Conditions: ADC clocked by falling edge, V_{OH_ADC} = VCC;
ECL CLK output type, V_{CLK} = 550mVp-p

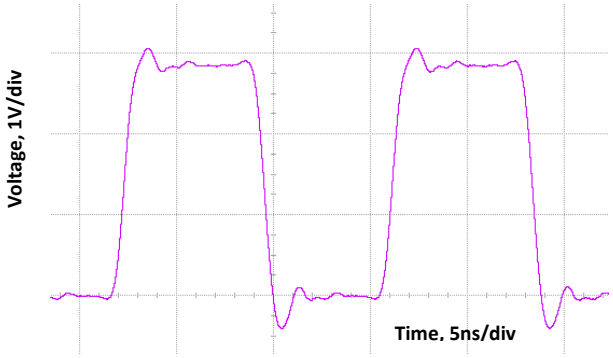


Figure 5.52: Typical clock output
Conditions: CMOS output type, V_{OH_CLK} = 2.85V, F_{CLK} = 72.27MHz

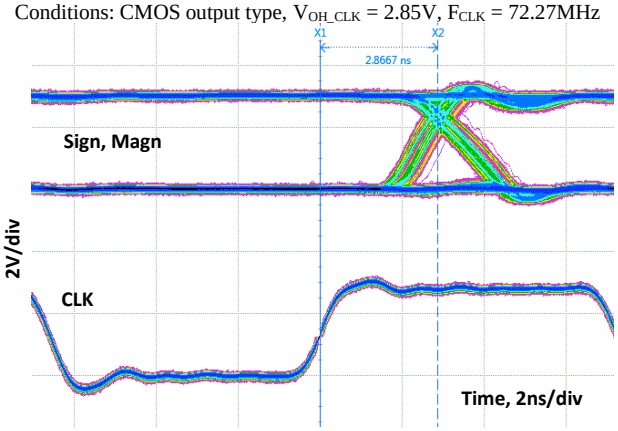


Figure 5.53: ADC output time diagram
Conditions: ADC clocked by rising edge, V_{OH_ADC} = VCC;
CMOS CLK output type, V_{OH_CLK} = 2.85V

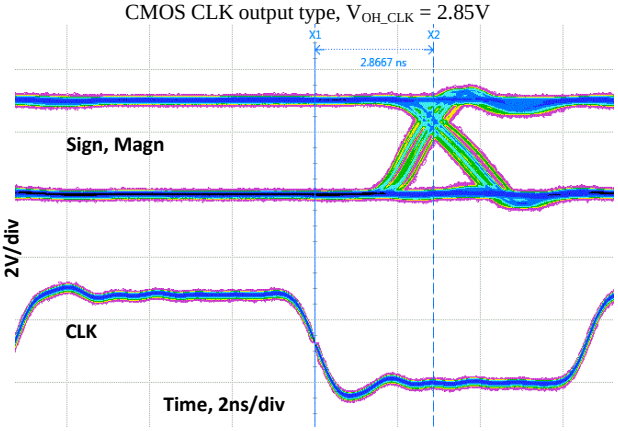


Figure 5.55: ADC output time diagram
Conditions: ADC clocked by falling edge, V_{OH_ADC} = VCC;
CMOS CLK output type, V_{OH_CLK} = 2.85V

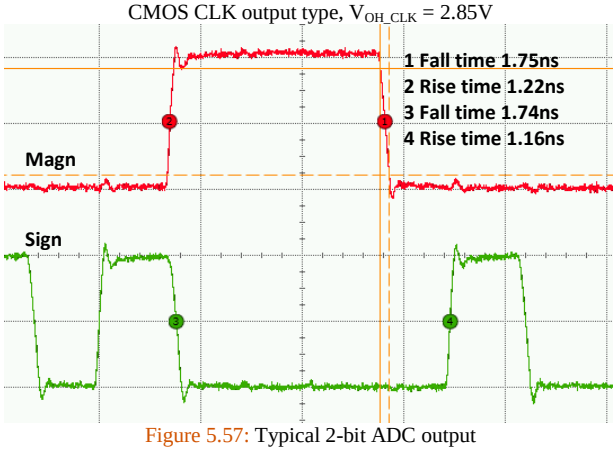


Figure 5.57: Typical 2-bit ADC output
Conditions: CMOS output without R_{LOAD}

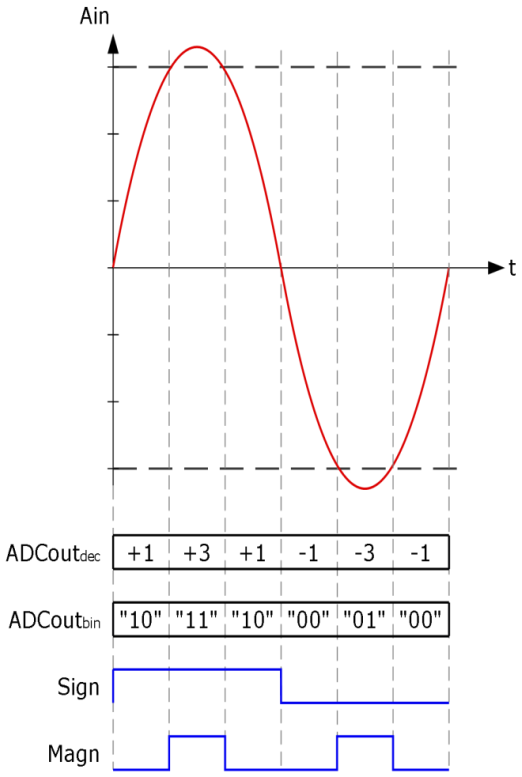


Figure 5.54: ADC quantization levels (sinewave signal example)

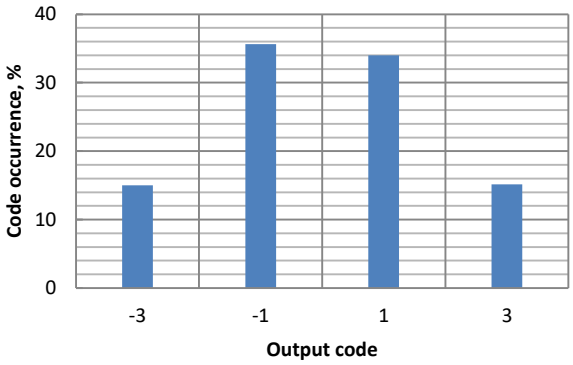


Figure 5.56: Channels “A”, “B”, “C” histogram
(2-bit ADC output)

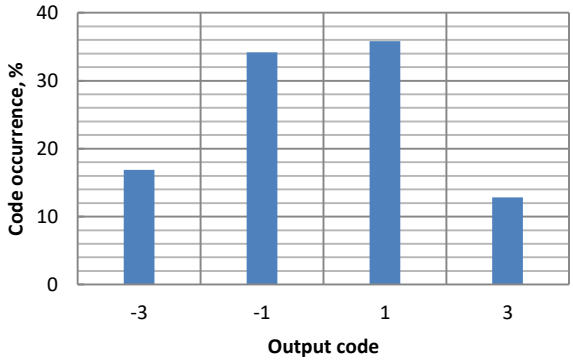


Figure 5.58: Channel “D” histogram
(2-bit ADC output)

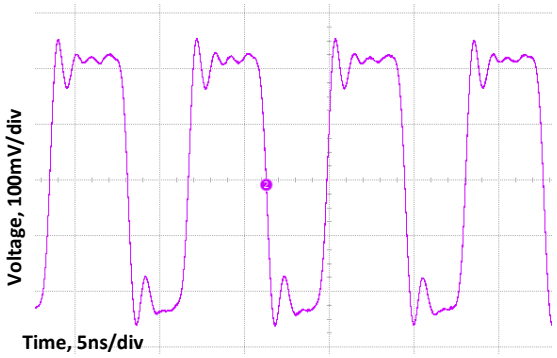


Figure 5.59 Clock output
Conditions: LVDS output type, R_{LOAD}=100Ohm,
V_{CLK} = 450mVp-p, F_{CLK} = 120MHz

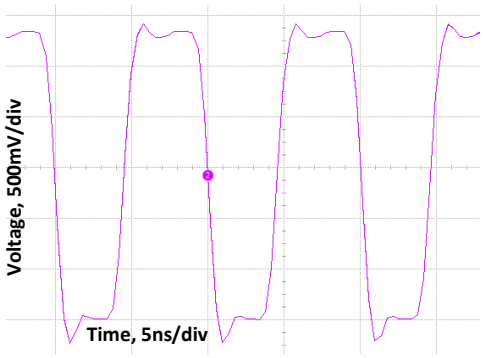


Figure 5.60 Clock output
Conditions: CMOS output type, V_{OH_CLK} = 2.85V, F_{CLK} = 100MHz

5.2. S-PARAMETERS

Please, open the attachment of the datasheet to download files with S-parameters. File names are given below.

Test conditions: V_{cc} = 3.0 V, T_a =+27°C. The effects of the test fixture have been de-embedded up to the pins of the device.

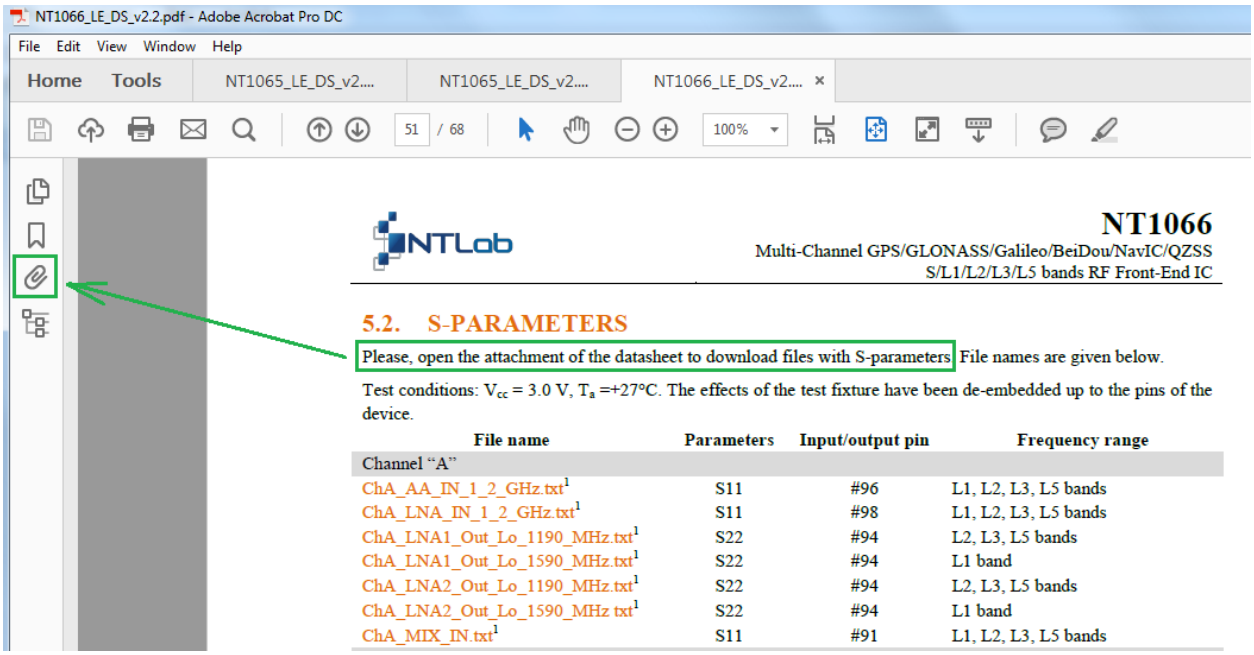
File name	Parameters	Input/output pin	Frequency range
Channel "A"			
ChA_AA_IN_1_2_GHz.txt[1]	S11	#96	L1, L2, L3, L5 bands
ChA_LNA_IN_1_2_GHz.txt[1]	S11	#98	L1, L2, L3, L5 bands
ChA_LNA1_Out_Lo_1190_MHz.txt[1]	S22	#94	L2, L3, L5 bands
ChA_LNA1_Out_Lo_1590_MHz.txt[1]	S22	#94	L1 band
ChA_LNA2_Out_Lo_1190_MHz.txt[1]	S22	#94	L2, L3, L5 bands
ChA_LNA2_Out_Lo_1590_MHz txt[1]	S22	#94	L1 band
ChA_MIX_IN.txt[1]	S11	#91	L1, L2, L3, L5 bands
Channel "B"			
ChB_AA_In_1_2_GHz.txt[1]	S11	#103	L1, L2, L3, L5 bands
ChB_LNA_In_1_2_GHz.txt[1]	S11	#101	L1, L2, L3, L5 bands
ChB_LNA1_Out_Lo_1190_MHz.txt[1]	S22	#105	L2, L3, L5 bands
ChB_LNA1_Out_Lo_1590_MHz.txt[1]	S22	#105	L1 band
ChB_LNA2_Out_Lo_1190_MHz.txt[1]	S22	#105	L2, L3, L5 bands
ChB_LNA2_Out_Lo_1590_MHz.txt[1]	S22	#105	L1 band
ChB_MIX_IN.txt[1]	S11	#108	L1, L2, L3, L5 bands
Channel "C"			
ChC_AA_In_1_2_GHz.txt[1]	S11	#14	L1, L2, L3, L5 bands
ChC_LNA_In_1_2_GHz.txt[1]	S11	#16	L1, L2, L3, L5 bands
ChC_LNA1_Out_Lo_1190_MHz.txt[1]	S22	#12	L2, L3, L5 bands
ChC_LNA1_Out_Lo_1590_MHz.txt[1]	S22	#12	L1 band
ChC_LNA2_Out_Lo_1190_MHz.txt[1]	S22	#12	L2, L3, L5 bands
ChC_LNA2_Out_Lo_1590_MHz.txt[1]	S22	#12	L1 band
ChC_MIX_IN.txt[1]	S11	#9	L1, L2, L3, L5 bands
Channel "D"			
ChD_DGPS_IN_balanced_65_110.txt[2]	S11	#22-23	FM band
ChD_DGPS_IN_balanced_160_240.txt[2]	S11	#22-23	VHF band
ChD_DGPS_IN_balanced_470.txt[2]	S11	#22-23	UHF band (lower range)
ChD_DGPS_IN_balanced_666.txt[2]	S11	#22-23	UHF band (central range)
ChD_DGPS_IN_balanced_862.txt[2]	S11	#22-23	UHF band (upper range)
ChD_IN_balanced.txt[2]	S11	#20-21	L2, L3, L5, S bands

Note 1: In order to uploaded files to different RF design environments or any software for viewing Touchstone (SnP) format their type should be changed to .s1p.
Note 2: In order to uploaded files to different RF design environments or any software for viewing Touchstone (SnP) format their type should be changed to .s2p. Pay attention, that input #1 is positive balanced signal, input #2 – negative balanced signal, reference ground is connected.

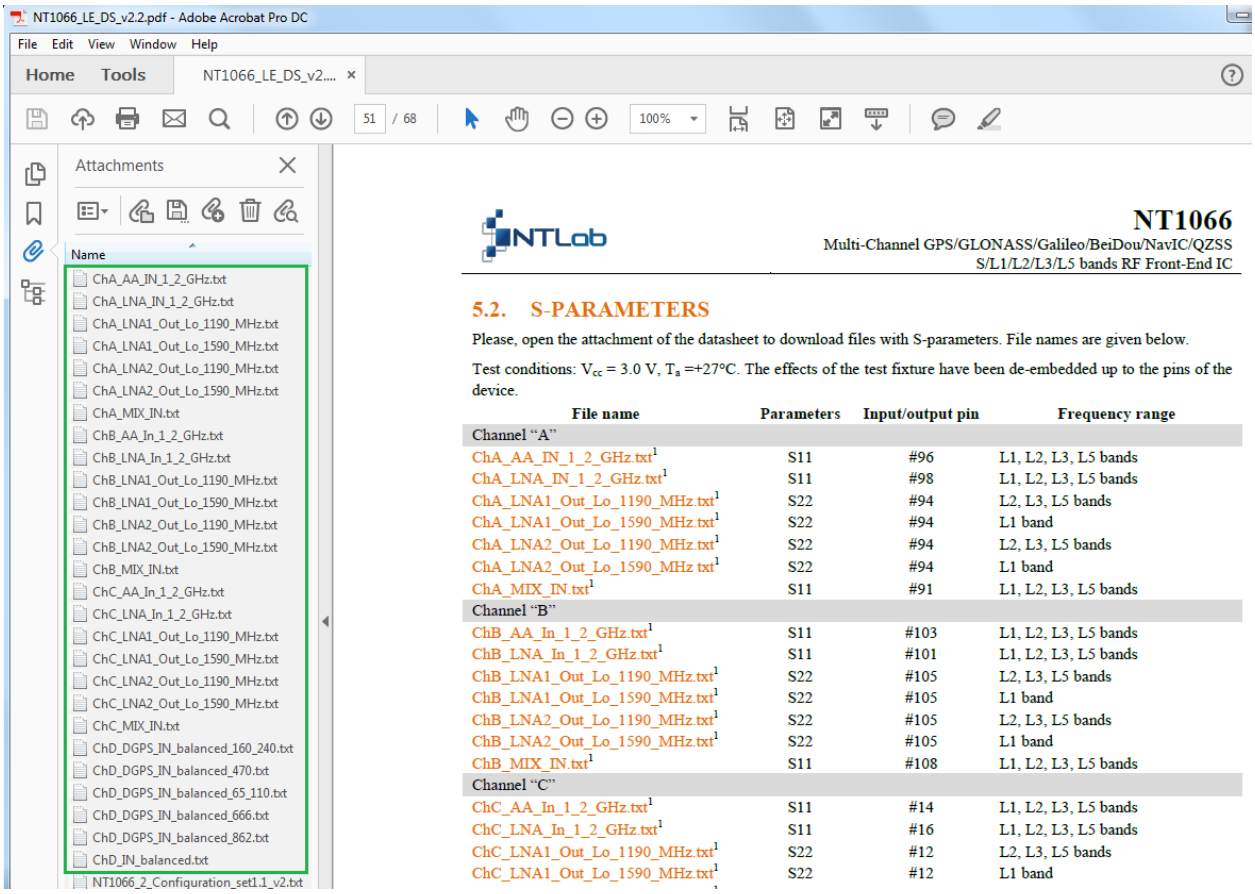
Typical S-parameters are provided "as they are" and with no warranty of any kind expressed or implied, including warranties of merchantability and fitness for a particular purpose.

To download any of attached files, follow instructions:

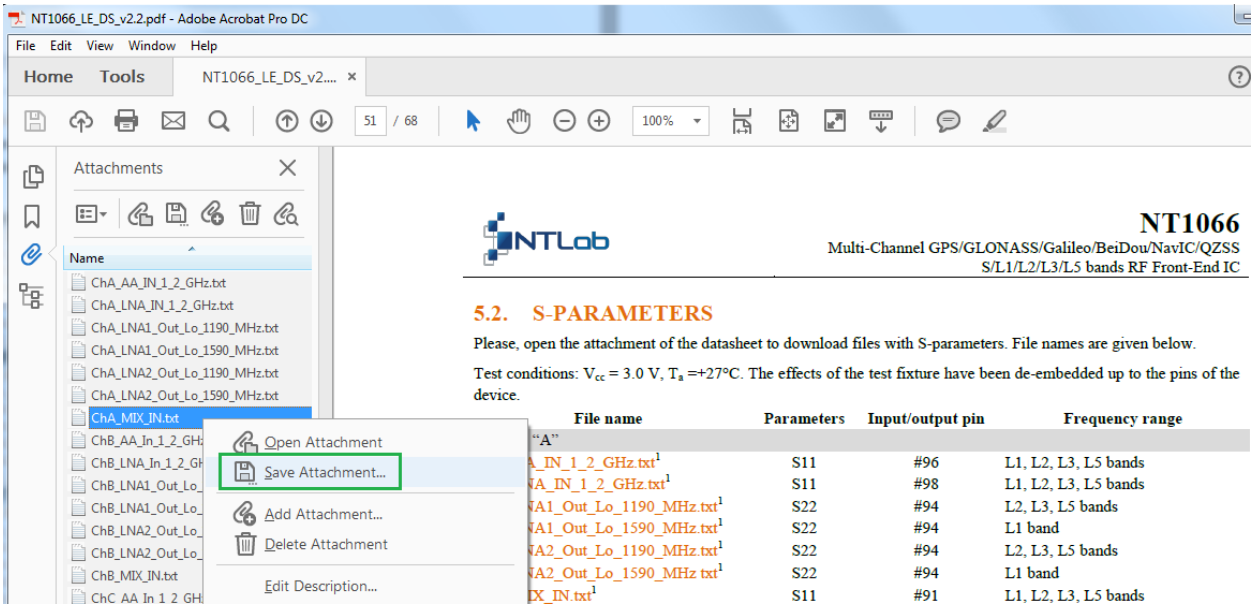
Step 1. Open datasheet in Adobe Acrobat and click on “Attachments”.



Step 2. The list of files will be available on the left.



Step 3. Right click to download the file.



5.3. IBIS MODEL

Please, open the attachment of the datasheet to download file “nt1066_ibis_v2.0.txt”.

Follow instructions from section 5.2 to download the model.

File may be also uploaded to different RF design environments or any software for viewing the electrical LUTs if renamed to *.ibs.

This IBIS model is provided as is and with no warranty of any kind expressed or implied, including warranties of merchantability and fitness for a particular purpose.

6. APPLICATION NOTES

Some tricks or not obvious actions as well as configuration examples are described in this section.

6.1. START UP PROCEDURE

NT1066 wakes up in shutdown mode: all channels and clock output are disabled. NT1066 can be reconfigured according to sequences given below. Make sure that output data interface comply with channel load and do not forget to execute PLL tuning and LPF autocalibration procedures. In order to activate chip one of the channels (Reg6 D[3–0]) or clock output (Reg6 D[4]) should be enabled.

6.2. REFERENCE FREQUENCY CONFIGURATION

NT1066 is preconfigured to 10MHz TCXO signal. If another TCXO is used, its value should be written to Reg7 D[7–0] + Reg8 D[7–0] to make NT1066 perform properly.

6.3. PLL RECONFIGURATION

NT1066 has the following preconfigures:

– PLL “A” is set to L1 band and feeds channel “A” with LO=1590MHz @ F_{TCXO}=10MHz
– PLL “B” is set to L2 band and feeds channel “B” with LO=1235MHz @ F_{TCXO}=10MHz
– PLL “C” is set to L3/L5 bands and feeds channel “C” with LO=1190MHz @ F_{TCXO}=10MHz
– PLL “D” is set to S band and feeds channel “D” with LO=2492MHz @ F_{TCXO}=10MHz

In order to reconfigure PLL “A”, “B” and “C” the following procedure is recommended:

– write LO frequency value to Reg17 D[6–0] + Reg18 D[7–0] + Reg19 D[7–0] for channel “A”, to Reg39 D[6–0] + Reg40 D[7–0] + Reg41 D[7–0] for channel “B” and to Reg61 D[6–0] + Reg62 D[7–0] + Reg63 D[7–0] for channel “C”
– choose PLL mode: integer-N or fractional-N in Reg20 D[0] for channel “A”, in Reg42 D[0] for channel “B” and in Reg64 D[0] for channel “C”
– if integer-N mode:
  - choose *R*, than *N* values according to the formula: $F_{LO} = \frac{F_{TCXO} \times N}{2R}$
  - write *R* value to Reg21 D[4–0] for channel “A”, to Reg43 D[4–0] for channel “B” and to Reg65 D[4–0] for channel “C”
  - write *N* value to Reg22 D[3–0] + Reg23 D[7–0] for channel “A”, to Reg44 D[3–0] + Reg45 D[7–0] for channel “B” and to Reg66 D[3–0] + Reg67 D[7–0] for channel “C”
– execute a tuning procedure in Reg24 D[0] for channel “A”, in Reg46 D[0] for channel “B” and in Reg68 D[0] for channel “C”

In order to reconfigure PLL “D” the following procedure is recommended:

– write LO frequency value to Reg87 D[6–0] + Reg88 D[7–0] + Reg89 D[7–0]
– execute a tuning procedure in Reg90 D[0]

It is necessary to run tuning procedure for each PLL if TCXO frequency was changed.

PLL lock indicator is available at Reg14 D[5] for channel “A”, at Reg35 D[5] for channel “B”, at Reg56 D[5] for channel “C” and at Reg80 D[0] for channel “D”.
Crossing of VCO voltage comparator upper threshold will be indicated by Reg14 D[4] for channel “A”, by Reg37 D[4] for channel “B”, by Reg60 D[4] for channel “C” and by Reg80 D[2] for channel “D”.
Crossing of VCO voltage comparator lower threshold will be indicated by Reg14 D[3] for channel “A”, by Reg36 D[3] for channel “B”, by Reg58 D[3] for channel “C” and by Reg80

D[1] for channel “D”.

6.4. PLL LOOP FILTER ADJUSTMENT

PLL loop filter should be adjusted if PFD frequency differs from default value. In this case the following registers values should be written to NT1066 depending on PFD frequency value.
If PLL loop filter was adjusted for not default conditions, default values must be overwritten to return to default state.

Channels “A”, “B” and “C”:

– PFD frequency ≤15MHz:
  - Reg125 x14 for channel “A” / Reg163 x14 for channel “B” / Reg201 x14 for channel “C”
  - Reg126 x14 for channel “A” / Reg164 x14 for channel “B” / Reg202 x14 for channel “C”
  - Reg127 x0E for channel “A” / Reg165 x0E for channel “B” / Reg203 x0E for channel “C”

  Note: *Default values.*

– PFD frequency >15MHz:
  - Reg125 x1F for channel “A” / Reg163 x1F for channel “B” / Reg201 x1F for channel “C”
  - Reg126 x1F for channel “A” / Reg164 x1F for channel “B” / Reg202 x1F for channel “C”
  - Reg127 x07 for channel “A” / Reg165 x07 for channel “B” / Reg203 x07 for channel “C”
  - Reg128 x00 for channel “A” / Reg166 x00 for channel “B” / Reg204 x00 for channel “C”

Channel “D”:

– PFD frequency ≤15MHz (S or L2/L3/L5 band):
  - Reg256 x04
  - Reg257 x04
  - Reg258 x0A

  Note: *Default values.*

– PFD frequency ≤15MHz (FM, VHF or UHF band):
  - Reg256 x0A
  - Reg257 x0A
  - Reg258 x07

– PFD frequency from 15MHz to 25MHz (all frequency bands):
  - Reg256 x14
  - Reg257 x14
  - Reg258 x03

– PFD frequency ≥25MHz (all frequency bands):
  - Reg256 x1F
  - Reg257 x1F
  - Reg258 x01

6.5. CHANNEL MODE CONFIGURATION

Channels “A”, “B” and “C” can operate in the following modes:

– IQ mode
– Upper sideband real mode
– Lower sideband real mode
– Lower sideband + upper sideband real mode

These modes can be set up in Reg16 D[1–0] for channel “A”, in Reg38 D[1–0] for channel “B”, Reg60 D[1–0] for channel “C”. Channels “A”, “B” and “C” are preconfigured to IQ mode.

Channel “D” operates only in IQ mode.

6.6. RF AGC CONFIGURATION

RF GC system of NT1066 in channel “D” starts into the manual operation mode (Reg91 D[1–0] is set to “00”). You can change RF gain value manually by setting a corresponding value with Reg91 D[6–3].

To enable the automatic mode Reg91 D[1–0] should be switched to “01”. In this case the RF GC system adjusts the RF gain to maintain operating in linear mode.

The status of RF gain is available at Reg81 D[3–0].

In order to control RF gain externally via pin #27, Reg91 D[1–0] should be switched to “10”. External controller output should be in Z-state when gain control mode is not external (when Reg91 D[1–0] is set to “00” or “01”).

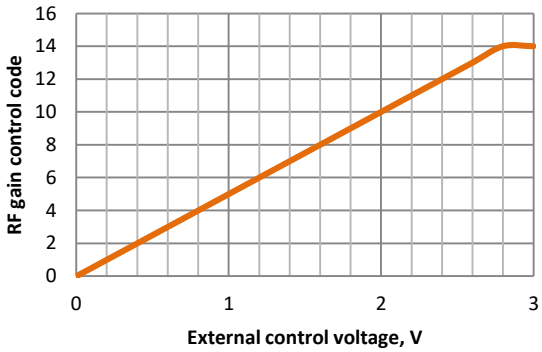


Figure 6.1: RF gain vs. external control voltage, Conditions: Channel “D”

6.7. LPF CALIBRATION

LPF autocalibration system is available for channels “A”, “B” and “C”. It is intended to compensate influence of temperature dependence and technological scatter on LPF characteristics. In Reg25 D[6–0] and Reg26 D[6–0] for channel “A”, Reg47 D[6–0] and Reg48 D[6–0] for channel “B”, Reg69 D[6–0] and Reg70 D[6–0] for channel “C” and Reg92 D[7–0] for channel “D” guaranteed range of LPF cut-off frequency is described for typical conditions. On marginal samples autocalibration system will compensate offset either in low-frequency range or in high-frequency range. After autocalibration you will get 3dB attenuation at the selected setting of guaranteed range for any chip in the specified temperature range.

LPF cut-off frequency should be the same for I and Q channels if IQ output type. If output type is real, LPF cut-off frequency can be different for upper and lower sideband.

It is necessary to execute LPF autocalibration procedure in Reg27 D[0] for channel “A”, in Reg49 D[0] for channel “B” and in Reg71 D[0] for channel “C” after chip activation, if LPF code or TCXO frequency were changed. LPF autocalibration system status is available in Reg14 D[0] for channel “A”, in Reg36 D[0] for channel “B” and in Reg58 D[0] for channel “C”.

6.8. IF AGC THRESHOLDS CONFIGURATION

IF GC system of NT1066 has the differences between the channels.

In channels “A”, “B” and “C” IF GC systems start into the auto operation mode with 2-bit ADC IF outputs. You can change digital detector threshold with respect to sinewave signal with Reg29 D[1–0] + Reg30 D[7–0] and Reg31 D[1–0] + Reg32 D[7–0] for channel “A”, Reg51 D[1–0] + Reg52 D[7–0] and Reg53 D[1–0] + Reg54 D[7–0] for channel “B” and Reg73 D[1–0] + Reg74 D[7–0] and Reg75 D[1–0] + Reg76 D[7–0] for channel “C”.

To enable manual mode write “1” to Reg28 D[1] for channel “A”, Reg50 D[1] for channel “B” and Reg72 D[1] for channel “C”. Then you can change IF gain value manually by setting a corresponding value with Reg29 D[1–0] + Reg30 D[7–0] and Reg31 D[1–0] + Reg32 D[7–0] for channel “A”, Reg51 D[1–0] + Reg52 D[7–0] and Reg53 D[1–0] + Reg54 D[7–0] for channel “B” and Reg73 D[1–0] + Reg74 D[7–0] and Reg75 D[1–0] + Reg76 D[7–0] for channel “C”.

In channel “D” IF GC system starts into the auto operation mode with 2-bit ADC IF outputs. While automatic mode is enabled, the IF AGC system adjusts the IF gain to keep its output power between IF AGC thresholds. You can change digital detector upper threshold with respect to sinewave signal with Reg98 D[7–0] and Reg100 D[7–0], lower threshold – with Reg99 D[7–0] and Reg101 D[7–0] .

For analog differential output type the thresholds correspond to the definite voltage level of the output stage. An upper threshold could be adjusted by Reg98 D[7–0] and Reg100 D[7–0]. A lower threshold could be adjusted by Reg99 D[7–0] and Reg101 D[7–0]. Voltage values shown in registers description (section 3.4.2.5) are calculated with respect to output signal power.

The upper threshold should always be higher than lower. Also it is strongly recommended to set a code value of upper threshold at least 5 codes higher than lower threshold to guarantee stability of IF AGC loop.

The IF AGC thresholds can be changed in order to achieve the desired output level for the subsequent ADC.

The status of IF gain control register is available in Reg82 D[0] + Reg83 D[7–0] and Reg84 D[0] + Reg85 D[7–0].

To enable manual mode the Reg93 D[1–0] should be switched to “0X”. You can change IF gain value manually by setting the corresponding value with Reg94 D[0] + Reg95 D[7–0] and Reg96 D[0] + Reg97 D[7–0].

To enable an external control mode via pins #38–39 Reg93 D[1–0] should be switched to “10”. External controller output should be in Z-state when gain control mode is not external (when Reg93 D[1–0] is set to “00”, “01” or “11”).

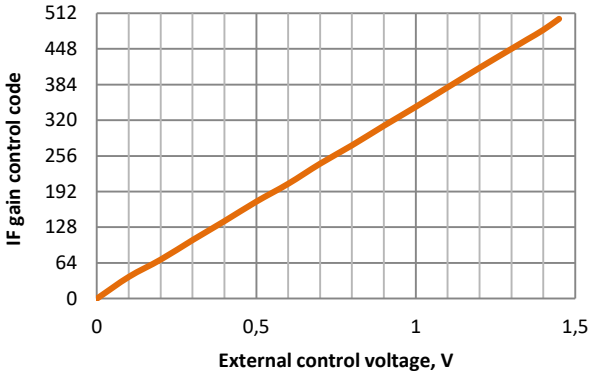


Figure 6.2: IF gain vs. external control voltage, Conditions: Channel “D”

6.9. OUTPUT DATA INTERFACE CONFIGURATION

After power up NT1066 is preconfigured to 2-bit ADC output data interface. However, there is an option to set up analog differential outputs in Reg28 D[0] for channel “A”, Reg50 D[0] for channel “B”, Reg72 D[0] for channel “C” and Reg93 D[2] for channel “D”.

2-bit ADCs are able to operate in one of three modes:
– asynchronous;
– clocked by falling edge;
– clocked by rising edge.

These modes can be set up in Reg28 D[5–4] for channel “A”, in Reg50 D[5–4] for channel “B”, in Reg72 D[5–4] for channel “C” and in Reg93 D[6–5] for channel “D”. For ADCs sampling frequency information, please, refer to subsection 6.11. In ‘asynchronous’ mode 2-bit ADCs act as voltage level comparators so no any clocking applied. For example, this mode may be useful if several NT1066s should operate simultaneously pushing out digitized data that can be synchronized with single clock on correlator and processor side.

2-bit ADCs output logic high level is configurable (available levels are 1.8V, 2.0V, 2.5V and VCC) and can be set with Reg28 D[3–2] for channel “A”, Reg50 D[3–2] for channel “B”, Reg72 D[3–2] for channel “C” and Reg93 D[4–3] for channel “D”.

6.10. ACTIVE ANTENNA DETECTION SYSTEM CONFIGURATION

Active antenna detection system is available in channels “A”, “B” and “C”.

Channels “A”, “B”, “C” can operate either with external active or passive antenna or without it. Active antenna detector is intended to detect whether active antenna is connected and whether its current is within acceptable thresholds. If current indicator is valid, you can change current consumption setting with Reg33 D[7–4] for channel “A”, with Reg55 D[7–4] for channel “B” and with Reg77 D[7–4] for channel “C”.

If active antenna current is four or more times lower than selected setting, active antenna connection status will be fail (available in Reg14 D[2] for channel “A”, in Reg36 D[2] for channel “B” and in Reg58 D[2] for channel “C”).

If active antenna current is two or more times higher than selected setting, active antenna current status will be fail (available in Reg14 D[1] for channel “A”, in Reg36 D[1] for channel “B” and in Reg58 D[1] for channel “C”).

Autoselection permission allows to select active LNA automatically if active antenna detector is enabled. LNA1 and LNA2 status are available in Reg14 D[7–6] for channel “A”, in Reg36 D[7–6] for channel “B” and in Reg58 D[7–6] for channel “C”.

In order to select required LNA manually the following registers should be switched to ‘0’: Reg34 D[3] for channel “A”, Reg56 D[3] for channel “B” and Reg78 D[3] for channel “C”. In this case you should firstly enable LNA in Reg34 D[1] for channel “A”, in Reg56 D[1] for channel “B” and in Reg78 D[1] for channel “C” and then select LNA type in Reg34 D[0] for channel “A”, in Reg56 D[0] for channel “B” and in Reg78 D[0].

There is an option to disable active antenna detector, it can be done in Reg34 D[2] for channel “A”, in Reg56 D[2] for channel “B” and in Reg78 D[2] for channel “C”. In this case LNA autoselection must be also disabled! You will have to select LNA manually according to the sequence given above.

If upper threshold of active antenna detector is exceeded, i.e. active antenna current is too high, detector can behave in two possible ways: limit current according to the upper threshold of current preset or limit current according to the upper threshold minimum possible preset. It is recommended to choose required preset in current limitation mode and then choose minimum current restriction mode if preferable. Active antenna detector behavior can be changed in Reg33 D[0] for channel “A”, in Reg55 D[0] for channel “B” and in Reg77 D[0] for channel “C”.

6.11. CLK FREQUENCY CONFIGURATION

CLK signal is intended for clocking all 2-bit ADCs as well as clocking external correlator engine. It can be generated from the following sources:

– LO frequency either from PLL “A” or PLL “B” or PLL “C” according to the formula: $F_{CLK} = F_{LO}/C$;
– reference signal pass-through;
– external sampling frequency via pins #52–53.

At default setup clock source is PLL “A”, clock frequency is set to 72.27MHz.

CLK source and frequency can be customized by procedure:

– choose CLK source by setting appropriate value to Reg10 D[2–0];
– write *C* value to Reg11 D[7–0] if PLL “A”, PLL “B” or PLL “C” source.

6.12. CLK OUTPUT TYPE USAGE

Clock output type is LVDS with configurable amplitude (refer to Reg12 D[6–5]) and can be used at clock frequencies up to 120MHz. Clock output type can be changed to CMOS (Reg10 D[4–3] = “00”) with configurable logic-level high (Reg12 D[2–0]) if clock frequency less than 100MHz is required. ECL (Reg10 D[4–3] = “01”) with configurable amplitude and DC level (Reg12 D[6–5] and D[4–3]) is not recommended for use if sharp falling and rising edges are required (see Figure 5.47, Figure 5.49 and Figure 5.51).

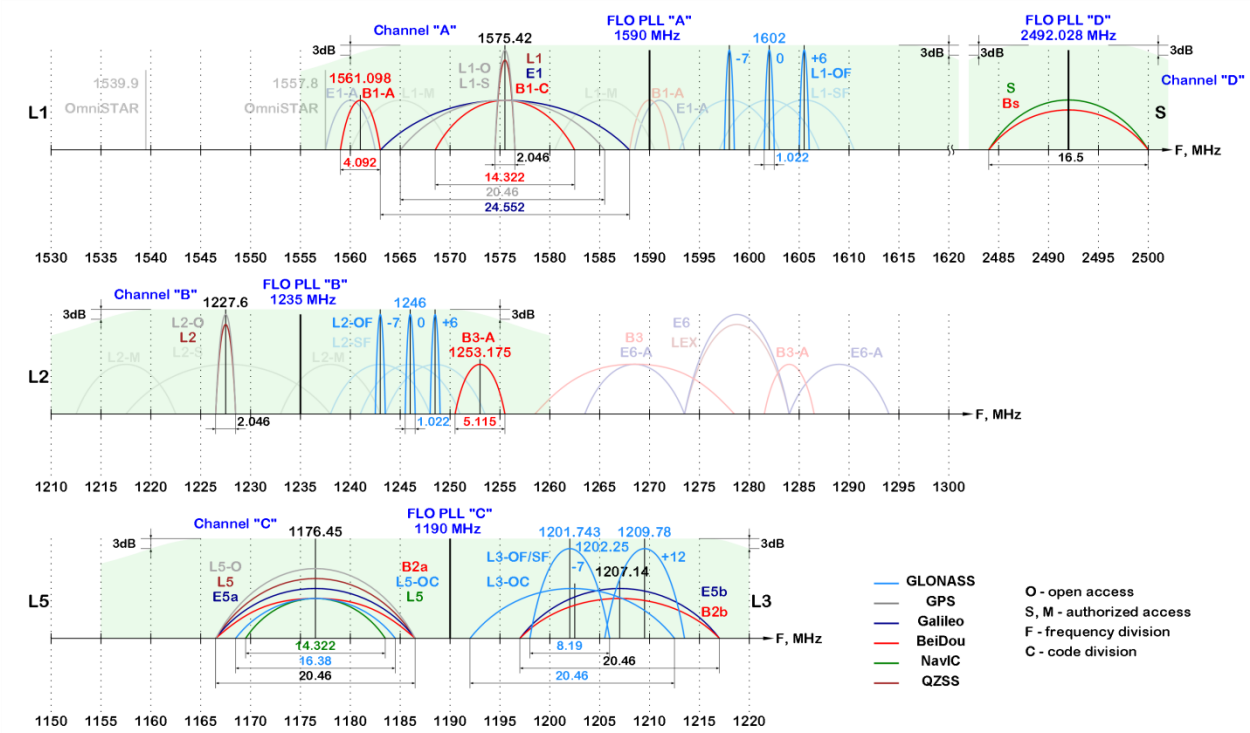
Choosing frequency plan, clock frequency, its output type and amplitude, pay attention to appearing of interferences at the Ch#_LNA_IN pins and then down converting to IF band. These interferences are caused by CLK signal harmonics and allocated frequencies can be calculated as $F_{jam} = N \times F_{CLK}, N = 1,2,3, \ldots$.

6.13. TEMPERATURE MEASUREMANT PROCEDURE

Two modes of temperature measurement are available: single and continuous (Reg9 D[1]). In single mode the measurement is done once upon request to Reg9 D[0] by setting “1” and result will be stored in Reg4 D[1–0] + Reg5 D[7–0] after procedure is finished (auto reset to “0” in Reg9 D[0] indicates this) until next execution. One temperature measurement procedure time is up to 17 ms. To enter in continuous mode set Reg9 D[1] to “1” first then execute with Reg9 D[0]. In this case embedded temperature sensor periodically runs the measurement procedure and only the latest result is stored in Reg4 D[1–0] + Reg5 D[7–0]. In order to stop continuous execution Reg9 D[1] should be set to “0”.

6.14. OPERATION EXAMPLES

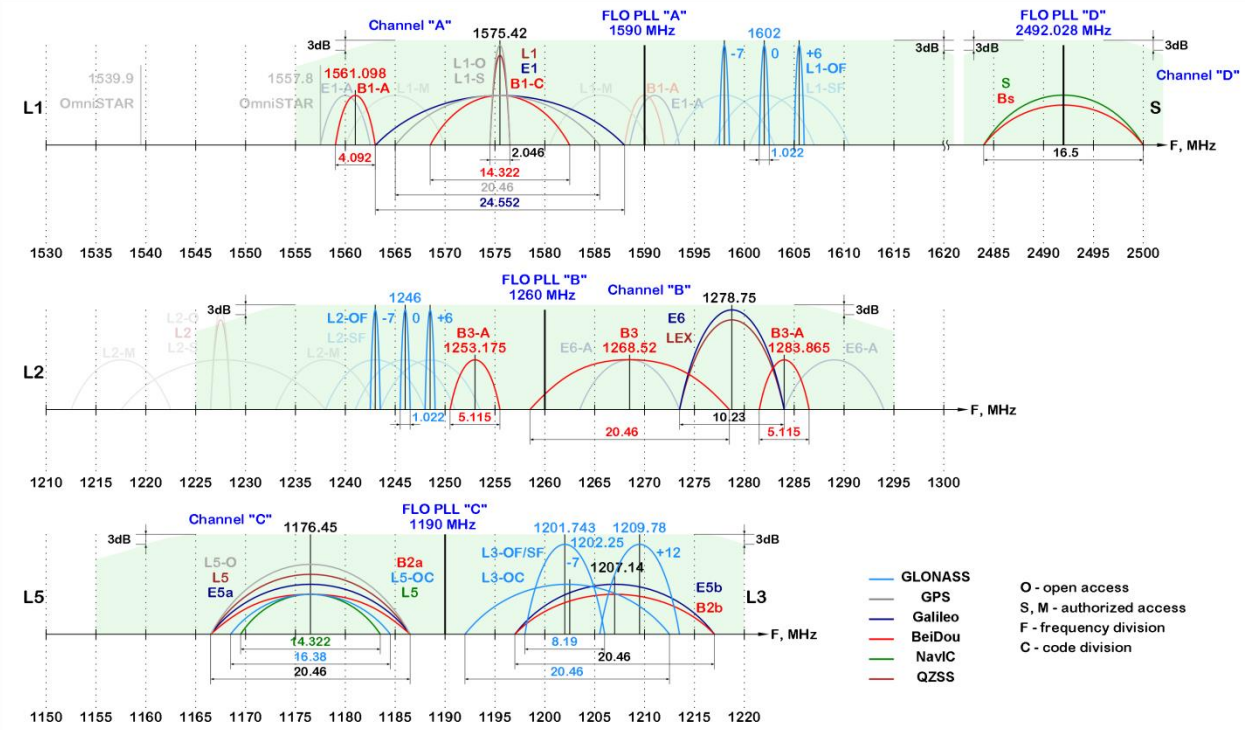
6.14.1. CONFIGURATION SET #1



General settings:		
Reference frequency	10 MHz	
CLK settings:		
CLK frequency source	PLL “A”	
CLK frequency	72.27 MHz	
CLK type	LVDS	
CLK amplitude	Preset 2	
PLL settings:		
F_{LO} PLL “A”	1590 MHz	
F_{LO} PLL “B”	1235 MHz	
F_{LO} PLL “C”	1190 MHz	
F_{LO} PLL “D”	2492 MHz	
Channel settings:		
Channel “A” GNSS	GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1	
Channel “B” GNSS	GPS L2, QZSS L2, GLONASS L2, BeiDou B3-A	
Channel “C” GNSS	GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, NavIC L5	
Channel “D” GNSS	NavIC S, BeiDou Bs	
Channel “A” IF passband	29.7 MHz	
Channel “B” IF passband	19.6 MHz	
Channel “C” IF passband	29.7 MHz	
Channel “D” IF passband	9.5 MHz	
GC mode:		
Channel “A”	IF auto	
Channel “B”	IF auto	
Channel “C”	IF auto	
Channel “D”	RF manual + IF auto	
Output data interface:	Configuration_set1.1	Configuration_set1.2
Channel “A”	2-bit ADC	analog differential
Channel “B”	2-bit ADC	analog differential
Channel “C”	2-bit ADC	analog differential
Channel “D”	2-bit ADC	analog differential
ADC output logic-level high	ext. (VCC)	–
ADC clock type	Clocked by falling edge	–

NT1066_Configuration_set1.X_vX.txt files are attached. Follow instructions from section 5.2 to download files. In order to use attached file under GUI its type should be changed to .hex.

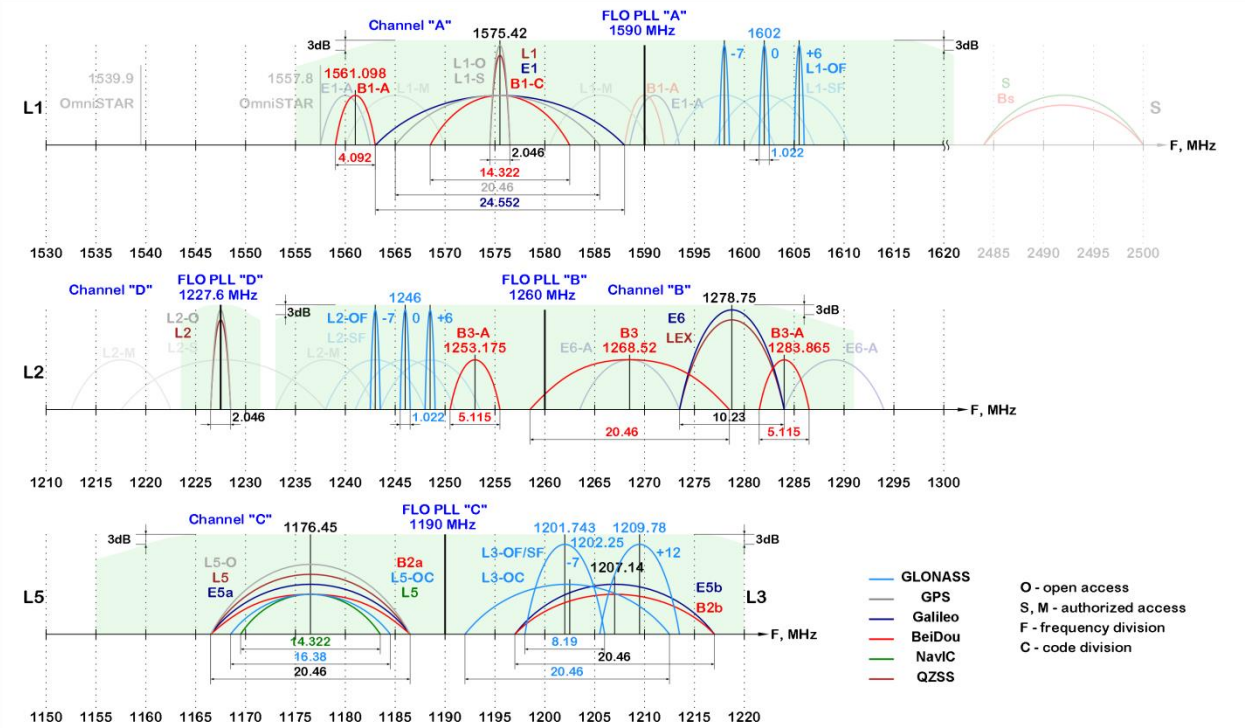
6.14.2. CONFIGURATION SET #2



General settings:	
Reference frequency	10 MHz
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	72.27 MHz
CLK type	LVDS
CLK amplitude	Preset 2
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1260 MHz
F_{LO} PLL “C”	1190 MHz
F_{LO} PLL “D”	2492 MHz
Channel settings:	
Channel “A” GNSS	GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1
Channel “B” GNSS	GLONASS L2, BeiDou B3, Galileo E6, QZSS LEX
Channel “C” GNSS	GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, NavIC L5
Channel “D” GNSS	NavIC S, BeiDou Bs
Channel “A” IF passband	29.7 MHz
Channel “B” IF passband	29.7 MHz
Channel “C” IF passband	29.7 MHz
Channel “D” IF passband	9.5 MHz
GC mode:	
Channel “A”	IF auto
Channel “B”	IF auto
Channel “C”	IF auto
Channel “D”	RF manual + IF auto
Output data interface:	
Channel “A”	2-bit ADC
Channel “B”	2-bit ADC
Channel “C”	2-bit ADC
Channel “D”	2-bit ADC
ADC output logic-level high	ext. (VCC)
ADC clock type	Clocked by falling edge

NT1066_Configuration_set2_vX.txt file is attached. Follow instructions from section 5.2 to download file. In order to use attached file under GUI its type should be changed to .hex.

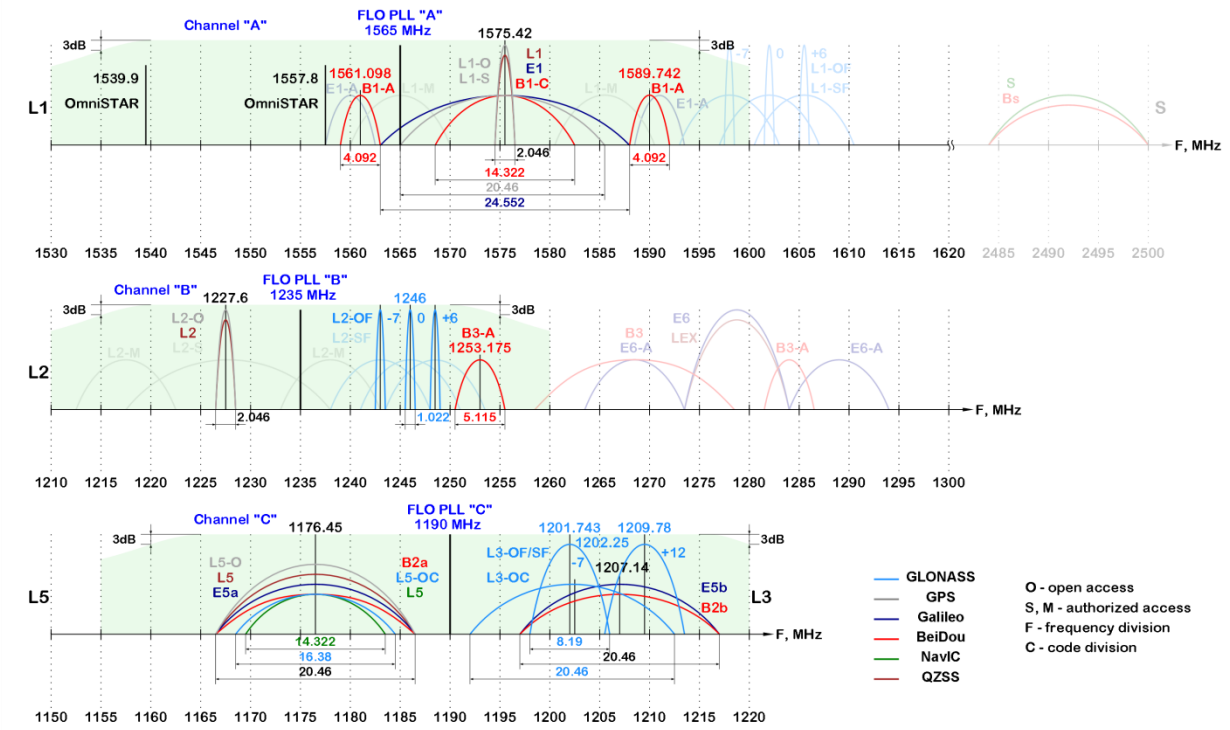
6.14.3. CONFIGURATION SET #3



General settings:	
Reference frequency	10 MHz
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	72.27 MHz
CLK type	LVDS
CLK amplitude	Preset 2
PLL settings:	
F_{LO} PLL “A”	1590 MHz
F_{LO} PLL “B”	1260 MHz
F_{LO} PLL “C”	1190 MHz
F_{LO} PLL “D”	1227.6 MHz
Channel settings:	
Channel “A” GNSS	GPS L1, QZSS L1, Galileo E1, BeiDou B1, GLONASS L1
Channel “B” GNSS	GLONASS L2, BeiDou B3, Galileo E6, QZSS LEX
Channel “C” GNSS	GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, NavIC L5
Channel “D” GNSS	GPS L2, QZSS L2
Channel “A” IF passband	29.7 MHz
Channel “B” IF passband	25.7 MHz
Channel “C” IF passband	29.7 MHz
Channel “D” IF passband	3.1 MHz
GC mode:	
Channel “A”	IF auto
Channel “B”	IF auto
Channel “C”	IF auto
Channel “D”	RF manual + IF auto
Output data interface:	
Channel “A”	2-bit ADC
Channel “B”	2-bit ADC
Channel “C”	2-bit ADC
Channel “D”	2-bit ADC
ADC output logic-level high	ext. (VCC)
ADC clock type	Clocked by falling edge

NT1066_Configuration_set3_vX.txt file is attached. Follow instructions from section 5.2 to download file. In order to use attached file under GUI its type should be changed to .hex.

6.14.4. CONFIGURATION SET #4



General settings:	
Reference frequency	10 MHz
CLK settings:	
CLK frequency source	PLL “A”
CLK frequency	71.14 MHz
CLK type	ECL
CLK DC level	Preset 4
CLK amplitude	Preset 2
PLL settings:	
F_{LO} PLL “A”	1565 MHz
F_{LO} PLL “B”	1235 MHz
F_{LO} PLL “C”	1190 MHz
F_{LO} PLL “D”	Unused
Channel settings:	
Channel “A” GNSS	OmniSTAR 1539.9, OmniSTAR 1557.8, BeiDou B1, GPS L1, Galileo E1, QZSS L1
Channel “B” GNSS	GPS L2, QZSS L2 , GLONASS L2, BeiDou B3-A
Channel “C” GNSS	GPS L5, GLONASS L3&L5, Galileo E5, QZSS L5, BeiDou B2, NavIC L5
Channel “D” GNSS	Unused
Channel “A” IF passband	29.7 MHz
Channel “B” IF passband	19.6 MHz
Channel “C” IF passband	29.7 MHz
Channel “D” IF passband	Unused
GC mode:	
Channel “A”	IF auto
Channel “B”	IF auto
Channel “C”	IF auto
Channel “D”	RF manual + IF auto
Output data interface:	
Channel “A”	2-bit ADC
Channel “B”	2-bit ADC
Channel “C”	2-bit ADC
Channel “D”	2-bit ADC
ADC output logic-level high	ext. (VCC)
ADC clock type	Clocked by falling edge

NT1066_Configuration_set4_vX.txt file is attached. Follow instructions from section 5.2 to download file. In order to use attached file under GUI its type should be changed to .hex.

6.15. PCB LAYOUT RECOMMENDATIONS

6.15.1. RECOMMENDED LAND PATTERN

NT1066 is easy-to-use and easy-to-implement solution where no special layout tricks required. Although common RF related layout techniques and information given below are recommended not to be ignored:

1. Analog power domain separated from digital domain is recommended to be allocated.
2. EMI-RFI shielding is highly recommended above NT1066 and related stuff.
3. Channels “A”, “B” and “C” input wave impedance should be 50Ohm for LNA1, LNA2 and mixer inputs (traces marked in green color).
4. Channel “D” (navigational input) input wave differential impedance should be 50Ohm (traces marked in light blue color).
5. Channel “D” (DGPS input) input wave differential impedance should be 100Ohm (traces marked in orange color). The same traces can be used for external sampling frequency differential input and clock frequency differential output.
6. Channels “A”, “B” and “C” output wave differential impedance can be in the range from 100Ohm to 510Ohm for analog output data interface (traces marked in yellow color).
7. Channel “D” output wave differential impedance can be in the range from 100Ohm to 1500Ohm for analog output data interface (traces marked in purple color).
8. To operate with maximum clock frequency (120MHz), corresponding traces should be as short as possible. Otherwise specified clock signal level is not guaranteed.

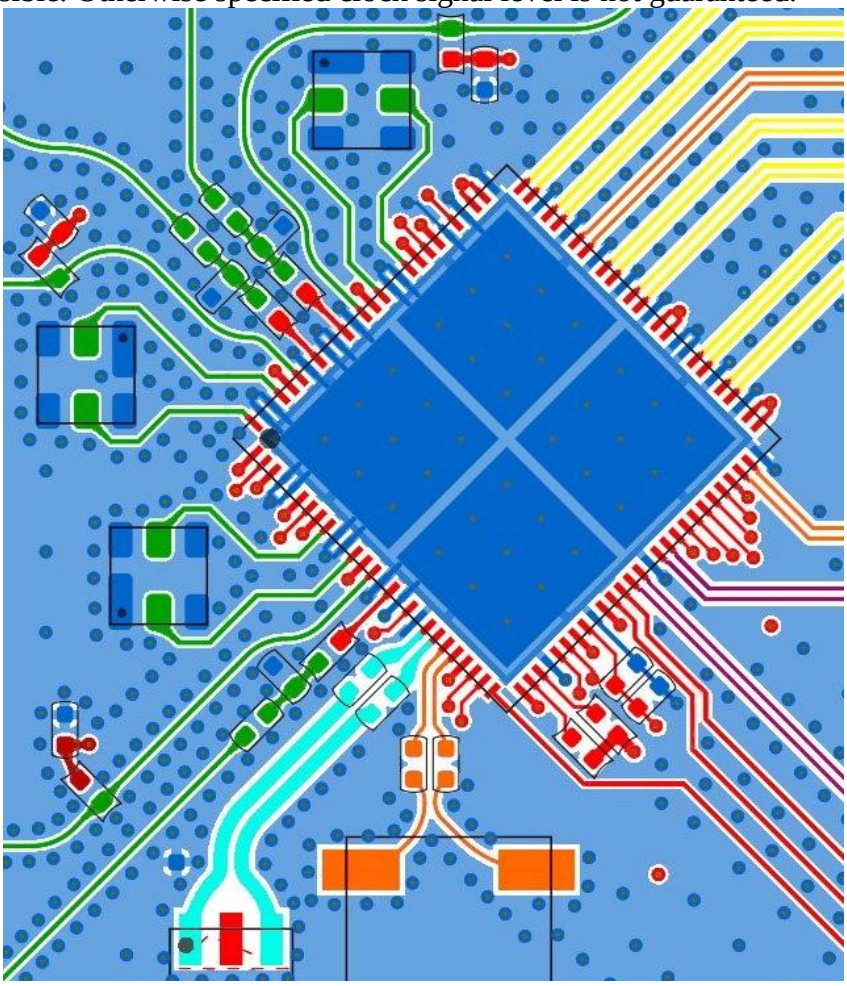
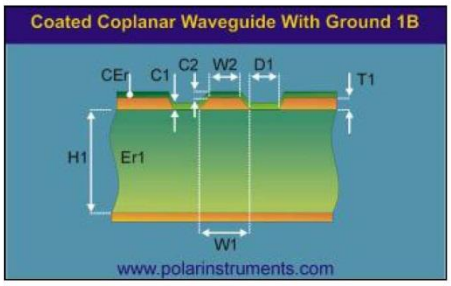


Figure 6.3: Recommended land pattern QFN108

6.15.2. ROGERS STACK UP

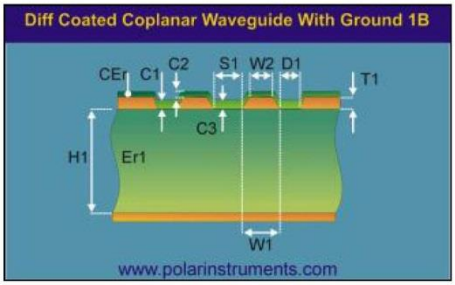
Rogers: Core RO4350B
R1755V High Tg 170: Core FR4 VK, PrePreg PP7628-45

NT1066 electrical characteristics given in sections 4 and 5 were proven on this very stack up.



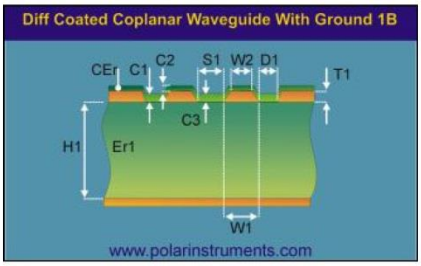
				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	0,1010	+/-	0,0000	0,1010	0,1010
Substrate 1 Dielectric	Er1	3,5500	+/-	0,0000	3,5500	3,5500
Lower Trace Width	W1	0,1700	+/-	0,0000	0,1700	0,1700
Upper Trace Width	W2	0,1450	+/-	0,0000	0,1450	0,1450
Ground Strip Separation	D1	0,0900	+/-	0,0000	0,0900	0,0900
Trace Thickness	T1	0,0180	+/-	0,0000	0,0180	0,0180
Coating Above Substrate	C1	0,0200	+/-	0,0000	0,0200	0,0200
Coating Above Trace	C2	0,0200	+/-	0,0000	0,0200	0,0200
Coating Dielectric	CEr	3,6000	+/-	0,0000	3,6000	3,6000
Impedance	Zo	49,54		------	0,00	0,00
Delay (ps/m)	D	5623,042		------	0,000	0,000
Inductance (nH/m)	L	278,566		------	0,000	0,000
Capacitance (pF/m)	C	113,505		------	0,000	0,000

Figure 6.4: 50Ohm traces calculation example



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	0,1010	+/-	0,0000	0,1010	0,1010
Substrate 1 Dielectric	Er1	3,5500	+/-	0,0000	3,5500	3,5500
Lower Trace Width	W1	0,1500	+/-	0,0000	0,1500	0,1500
Upper Trace Width	W2	0,1400	+/-	0,0000	0,1400	0,1400
Trace Separation	S1	0,1700	+/-	0,0000	0,1700	0,1700
Ground Strip Separation	D1	0,1400	+/-	0,0000	0,1400	0,1400
Trace Thickness	T1	0,0180	+/-	0,0000	0,0180	0,0180
Coating Above Substrate	C1	0,0200	+/-	0,0000	0,0200	0,0200
Coating Above Trace	C2	0,0200	+/-	0,0000	0,0200	0,0200
Coating Between Traces	C3	0,0200	+/-	0,0000	0,0200	0,0200
Coating Dielectric	CEr	3,6000	+/-	0,0000	3,6000	3,6000
Differential Impedance	Zdiff	100,67		------	0,00	0,00
Delay (Odd Mode) (ps/m)	D	5521,582		------	0,000	0,000
Odd Mode Impedance	Zodd	50,34		------	0,00	0,00
Even Mode Impedance	Zeven	61,17		------	0,00	0,00
Common Mode Impedance	Zcommon	30,58		------	0,00	0,00

Figure 6.5: 100Ohm differential traces calculation example



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	0,1010	+/-	0,0000	0,1010	0,1010
Substrate 1 Dielectric	Er1	3,5500	+/-	0,0000	3,5500	3,5500
Lower Trace Width	W1	0,5000	+/-	0,0000	0,5000	0,5000
Upper Trace Width	W2	0,4750	+/-	0,0000	0,4750	0,4750
Trace Separation	S1	0,1500	+/-	0,0000	0,1500	0,1500
Ground Strip Separation	D1	0,1500	+/-	0,0000	0,1500	0,1500
Trace Thickness	T1	0,0180	+/-	0,0000	0,0180	0,0180
Coating Above Substrate	C1	0,0250	+/-	0,0000	0,0250	0,0250
Coating Above Trace	C2	0,0250	+/-	0,0000	0,0250	0,0250
Coating Between Traces	C3	0,0250	+/-	0,0000	0,0250	0,0250
Coating Dielectric	CEr	3,6000	+/-	0,0000	3,6000	3,6000

Differential Impedance	Zdiff	50,05	------	50,05	50,05
Delay (Odd Mode) (ps/m)	D	5713,246	------	5713,246	5713,246
Odd Mode Impedance	Zodd	25,02	------	25,02	25,02
Even Mode Impedance	Zeven	29,16	------	29,16	29,16
Common Mode Impedance	Zcommon	14,58	------	14,58	14,58

Figure 6.6: 50Ohm differential traces calculation example

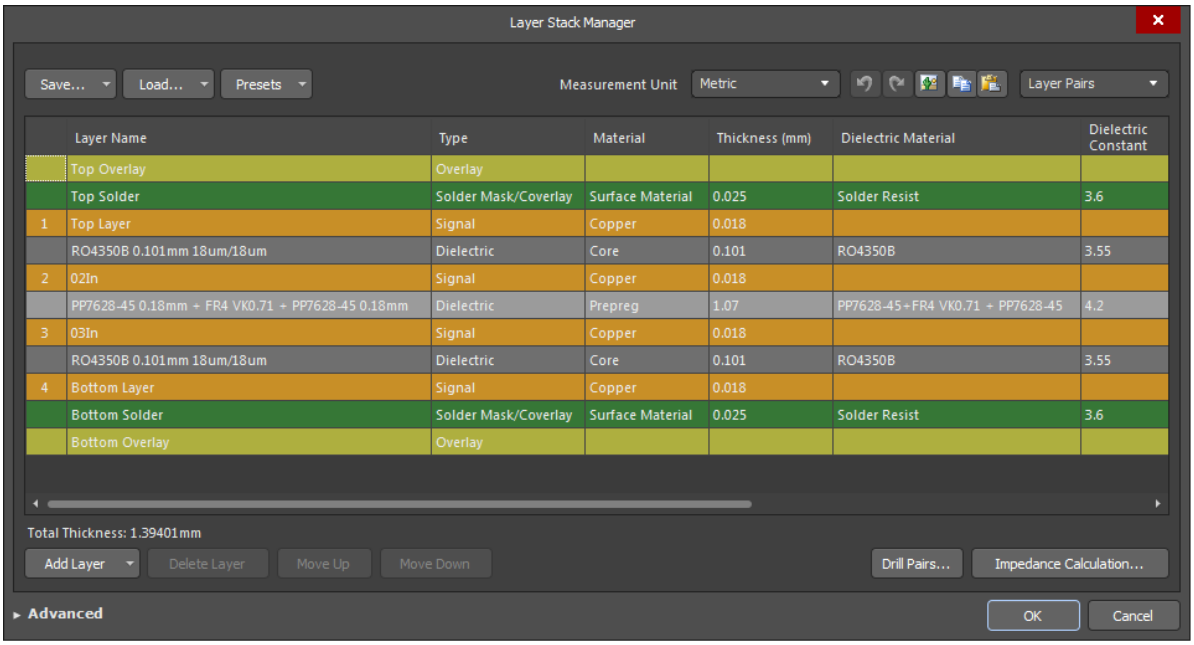


Figure 6.7: Layer stack manager example

7. PACKAGE INFORMATION

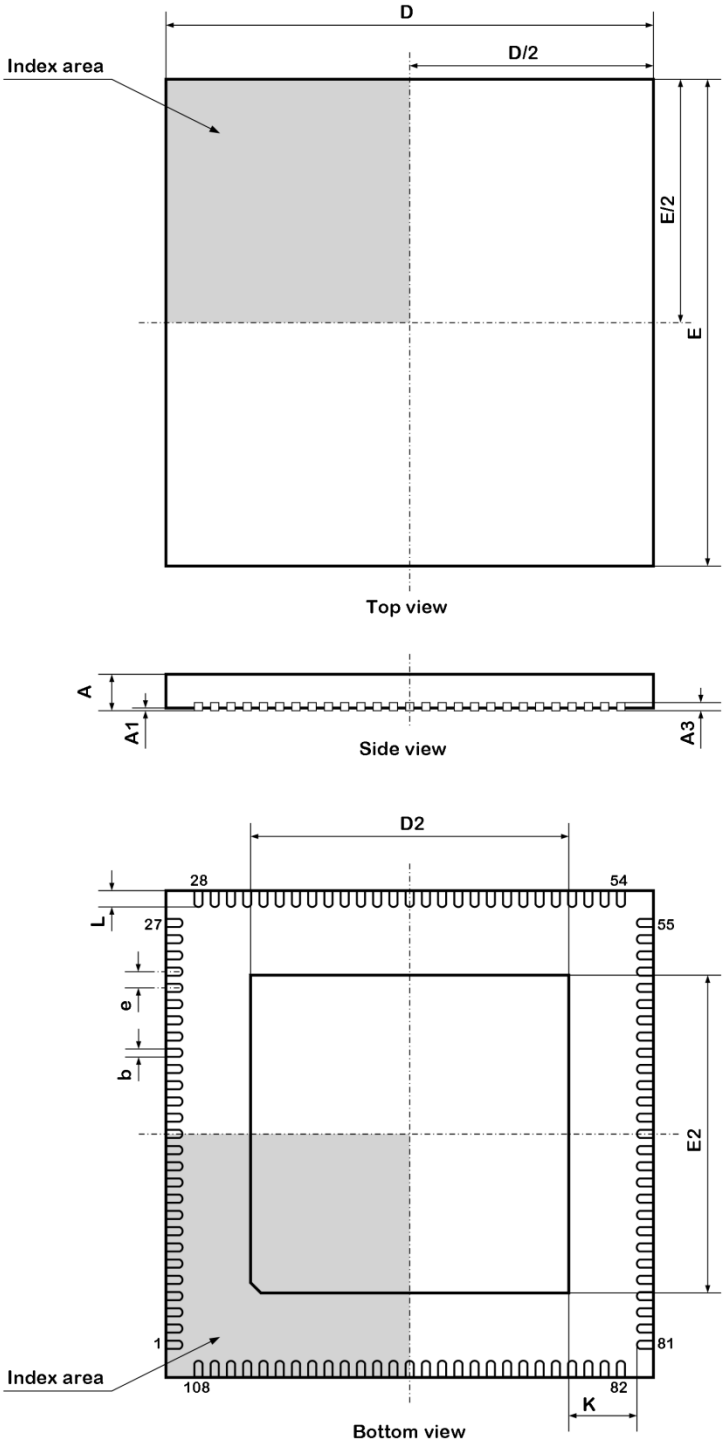


Figure 7.1: Package QFN108 12×12[1]

Table 7.1: Package QFN108 12×12 dimension[1]

Unit	A	A1	A3	b	D	D2	E	E2	e	K	L
min, mm	0.80	0.00		0.15		7.75		7.75		0.20	0.35
typ., mm	0.85	0.02	0.203	0.20	12.00	7.80	12.00	7.80	0.40	–	0.40
max, mm	0.90	0.05		0.25		7.85		7.85		–	0.45

Note 1: Package drawing and dimensions are for reference only. Actual values are compliant to JEDEC standard outlines MO–220.

8. ORDERING INFORMATION

For further information about this product, development roadmap, availability and licensing terms, please e-mail to sales@ntlab.com with ordering code “NT1066”.

9. REVISION HISTORY

From version 2.3 to 2.4:

- Valid chip versions are 1066.2 or 1066.3. Versions have **no differences** in operating characteristics. Version 1066.1 is obsolete.

From version 2.2 to 2.3:

- Subsection 5.2 “S-parameters”: instructions on downloading attached files were added.
- Subsection 6.15.1 “PCB layout recommendations”: Figure 6.3 “Recommended land pattern QFN108” updated

From version 2.1 to 2.2:

- Subsection 3.4.2.3 “CLK settings”: Reg10 and Reg12 description updated.
- Section 4 “Operating characteristics” updated:
  - Subsection 4.2 “AC electrical characteristics”: CMOS clock maximum frequency changed to 100MHz.
  - Subsection 4.2.1 “Channels “A”, “B”, “C” AC electrical characteristics”: total maximum gain, LNA1 gain and LNA2 gain typical values splitted for L1 band and L2/L3/L5 band.
- Section 5 “Typical characteristics” updated:
  - Subsection 5.1 “Typical characteristics”: Figure 5.31, Figure 5.59 and Figure 5.60 added.
  - Subsection 5.3 “IBIS model” added.
- Subsection 6.12 “CLK output type usage”: application notes updated.

From version 2.0 to 2.1:

- Subsection 3.4.2 “Programmable registers” updated:
  - Reg28, Reg50, Reg72 D[5–4] and Reg93 D[6–5]: ADC clock types description updated
  - Reg91 D[6–3]: RF gain control values updated
- Section 4 “Operating characteristics” updated for NT1066.2.
- Section 5 “Typical characteristics” updated for NT1066.2.
- Subsection 6.14 “Operation examples”: updated description for Reg28, Reg50, Reg72, Reg91, Reg93.

Updates and modifications from version NT1066.1 (refer to Reg0 and Reg1 for chip number and version):

- Default fix no longer needed.
- Subsection 3.2.2, Figure 3.4 added: Channel “A” specific application schematic if channel is not used.
- Subsection 3.4.2 “Programmable registers” updated:
  - Reg1 D[2–0]: Chip version changed to 2.
  - Reg3 D[0]: channel “D” cumulative status AOK control logic updated.
  - Reg10 D[4–3]: LVDS clock output type available.
  - Reg12 D[6–5]: LVDS clock amplitude setting available.
  - Reg12 D[4–3]: ECL clock output DC level setting available.
  - Reg12 D[2–0]: CMOS clock output logic-level high setting available.

  - Reg28, Reg50, Reg72 D[5–4] and Reg93 D[6–5]: ADC type (synchronous or asynchronous) doesn't depend on clock output type.
  - Reg28, Reg50, Reg72 D[1–0]: IFA gain control mode and output data interface settings separated. Control logic was changed, only default mode matches with NT1066.1. 2-bit ADC output with manual gain control mode is available.
  - Reg99 and Reg101: default values changed from x4C to x46.
- Section 4 "Operating characteristics" updated for NT1066.2.
  - Channel "D" operating temperature range is up to +85°C.
- Section 5 "Typical characteristics" updated for NT1066.2.
- Section 6 "Application notes:
  - Default fix no longer needed.
  - Subsection 6.4 "PLL loop filter adjustment" updated.
  - Subsection 6.12 "CLK output type usage" updated.
  - Subsection 6.14 "Operation examples" updated.